What could possibly go wrong with <insert x86 instruction here>?

Clémentine Maurice, Moritz Lipp

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Who we are

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→ cache attacks without memory accesses and bypassing kernel ASLR

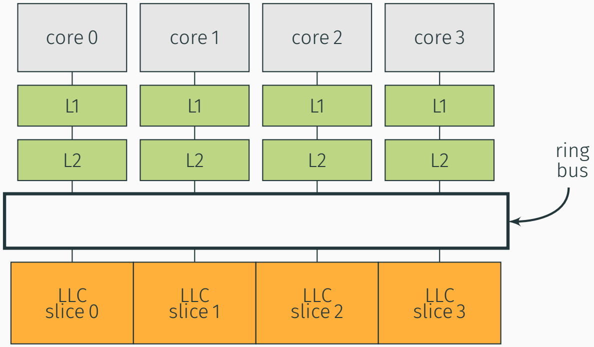
→ cache attacks can also be mounted on ARM, not solely on x86

Outline

- Background
- `mov` — The beginning of cache attacks
- `clflush` — Cache attacks without memory accesses
- `prefetch` — Lost in translation
- Bonus track — Even more instructions, even more attacks

Introduction

Caches on Intel CPUs



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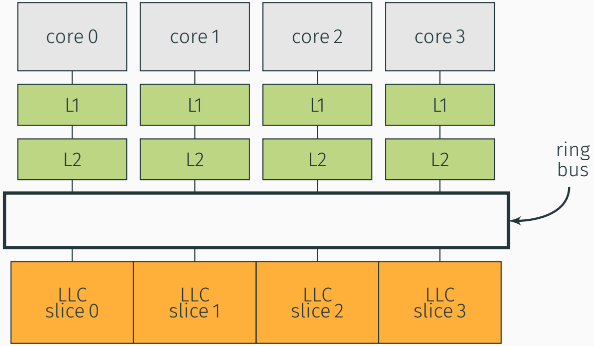
Caches on Intel CPUs



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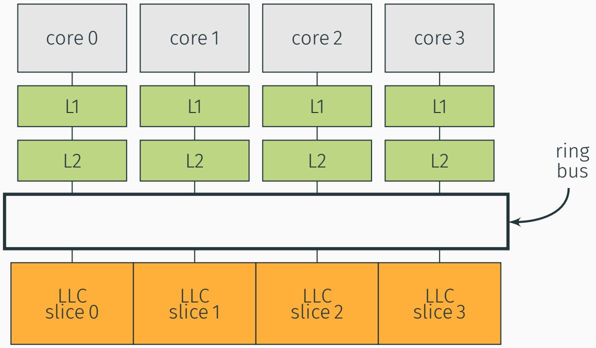

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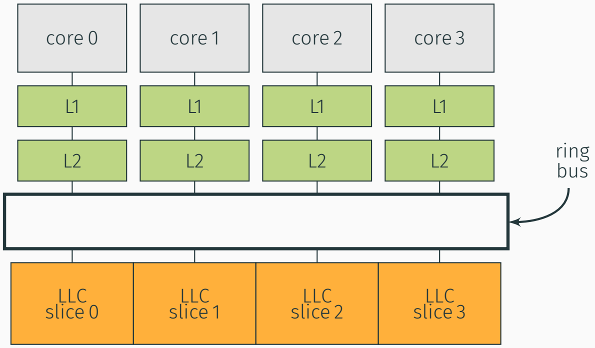

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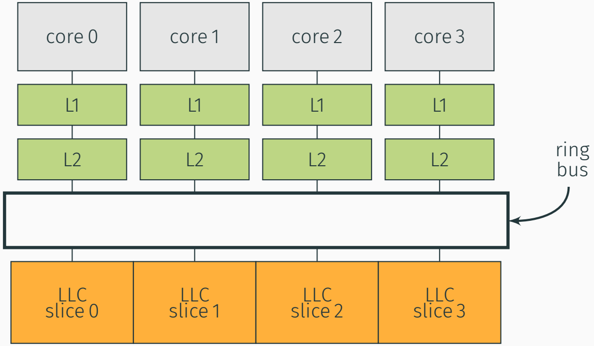

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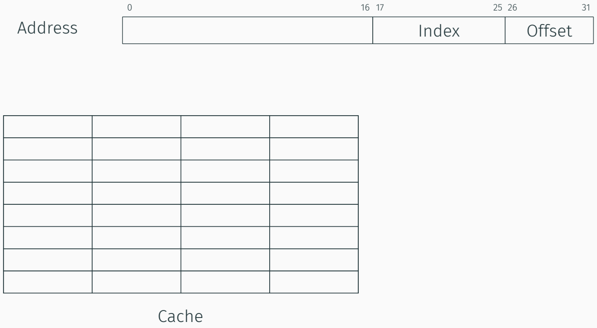
    - inclusive

Set-associative caches



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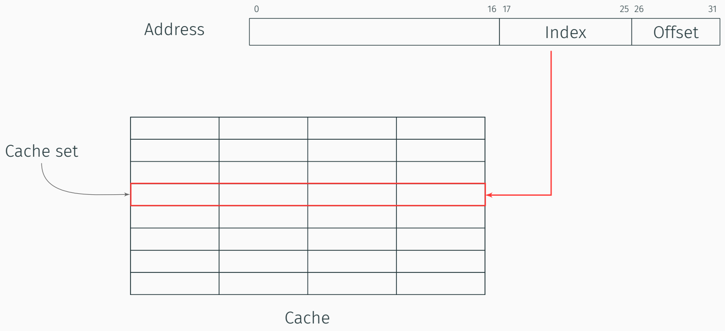

Data loaded in a specific set depending on its address

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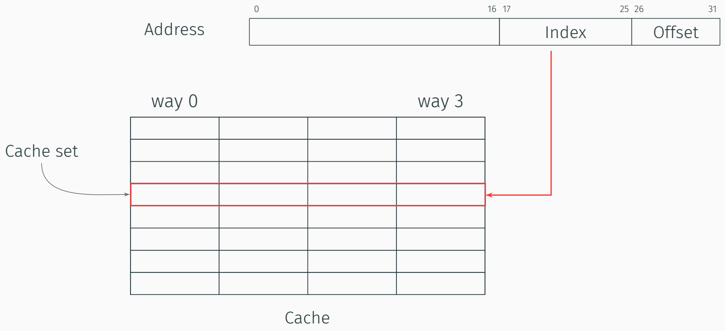

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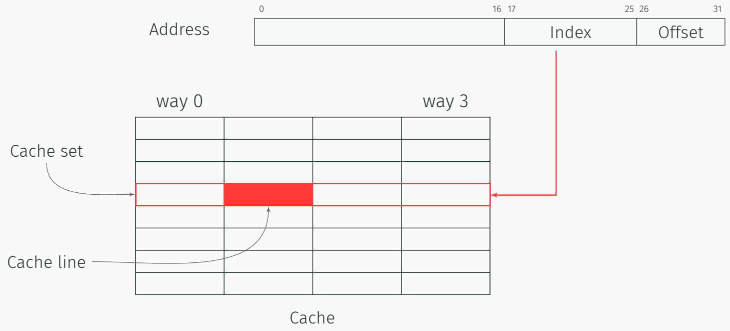

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Cache line loaded in a specific way depending on the replacement policy

Today’s menu

Three instructions

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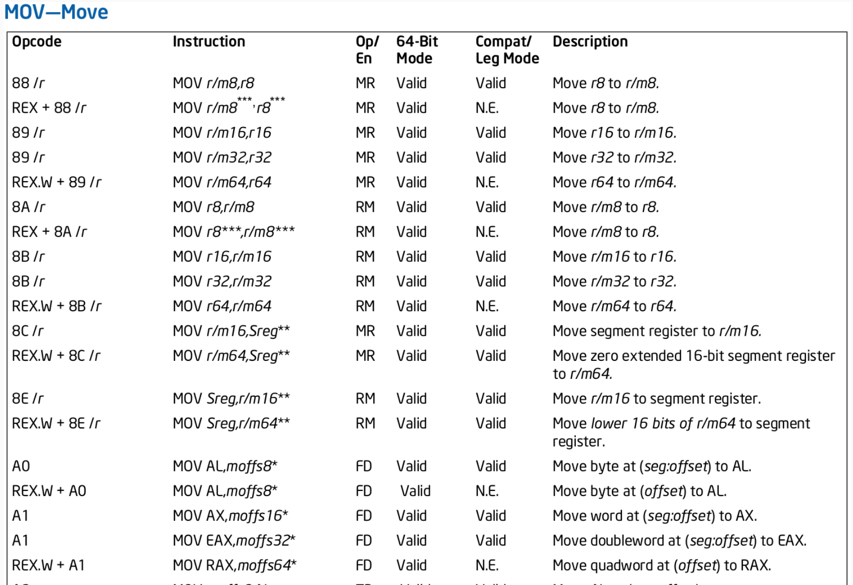
That's all the assembly you need for today!

mov

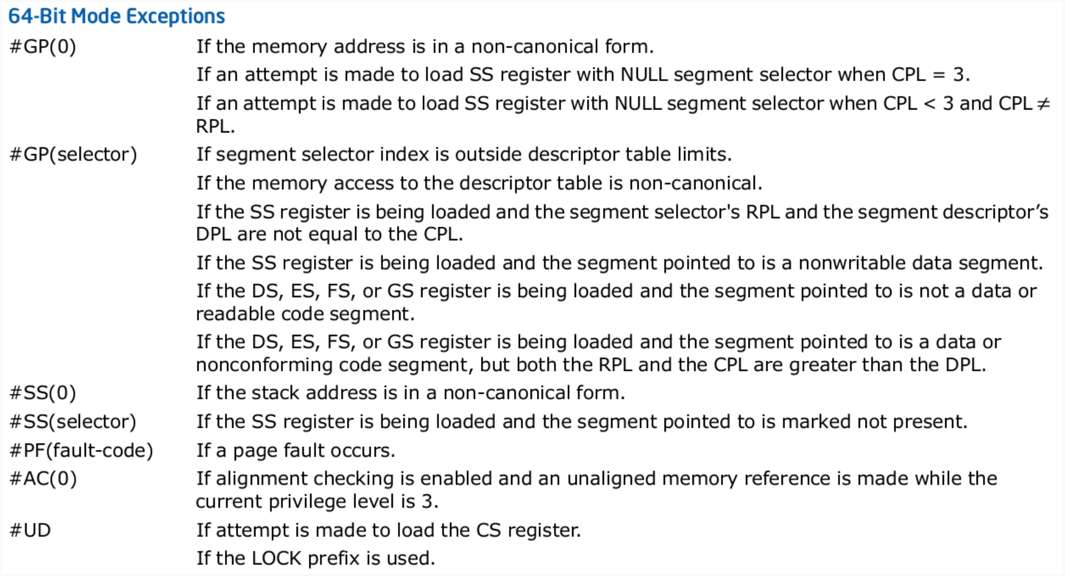
mov



MOV—Move

Opcode	Instruction	Op/ En	64-Bit Mode	Compat/ Leg Mode	Description
88 */r*	MOV *r/m8,r8*	MR	Valid	Valid	Move *r8* to *r/m8.*
REX + 88 */r*	MOV *r/m8***,r8****	MR	Valid	N.E.	Move *r8* to *r/m8.*
89 */r*	MOV *r/m16,r16*	MR	Valid	Valid	Move *r16* to *r/m16.*
89 */r*	MOV *r/m32,r32*	MR	Valid	Valid	Move *r32* to *r/m32.*
REX.W + 89 */r*	MOV *r/m64,r64*	MR	Valid	N.E.	Move *r64* to *r/m64.*
8A */r*	MOV *r8,r/m8*	RM	Valid	Valid	Move *r/m8* to *r8.*
REX + 8A */r*	MOV *r8***,r/m8****	RM	Valid	N.E.	Move *r/m8* to *r8.*
8B */r*	MOV *r16,r/m16*	RM	Valid	Valid	Move *r/m16* to *r16.*
8B */r*	MOV *r32,r/m32*	RM	Valid	Valid	Move *r/m32* to *r32.*
REX.W + 8B */r*	MOV *r64,r/m64*	RM	Valid	N.E.	Move *r/m64* to *r64.*
8C */r*	MOV *r/m16,Sreg***	MR	Valid	Valid	Move segment register to *r/m16.*
REX.W + 8C */r*	MOV *r/m64,Sreg***	MR	Valid	Valid	Move zero extended 16-bit segment register to *r/m64.*
8E */r*	MOV *Sreg,r/m16***	RM	Valid	Valid	Move *r/m16* to segment register.
REX.W + 8E */r*	MOV *Sreg,r/m64***	RM	Valid	Valid	Move *lower 16 bits of r/m64* to segment register.
A0	MOV AL,*moffs8**	FD	Valid	Valid	Move byte at (*seg:offset*) to AL.
REX.W + A0	MOV AL,*moffs8**	FD	Valid	N.E.	Move byte at (*offset*) to AL.
A1	MOV AX,*moffs16**	FD	Valid	Valid	Move word at (*seg:offset*) to AX.
A1	MOV EAX,*moffs32**	FD	Valid	Valid	Move doubleword at (*seg:offset*) to EAX.
REX.W + A1	MOV RAX,*moffs64**	FD	Valid	N.E.	Move quadword at (*offset*) to RAX.

mov



64-Bit Mode Exceptions

#GP(0)	If the memory address is in a non-canonical form.
	If an attempt is made to load SS register with NULL segment selector when CPL = 3.
	If an attempt is made to load SS register with NULL segment selector when CPL < 3 and CPL ≠ RPL.
#GP(selector)	If segment selector index is outside descriptor table limits.
	If the memory access to the descriptor table is non-canonical.
	If the SS register is being loaded and the segment selector's RPL and the segment descriptor’s DPL are not equal to the CPL.
	If the SS register is being loaded and the segment pointed to is a nonwritable data segment.
	If the DS, ES, FS, or GS register is being loaded and the segment pointed to is not a data or readable code segment.
	If the DS, ES, FS, or GS register is being loaded and the segment pointed to is a data or nonconforming code segment, but both the RPL and the CPL are greater than the DPL.
#SS(0)	If the stack address is in a non-canonical form.
#SS(selector)	If the SS register is being loaded and the segment pointed to is marked not present.
#PF(fault-code)	If a page fault occurs.
#AC(0)	If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD	If attempt is made to load the CS register.
	If the LOCK prefix is used.

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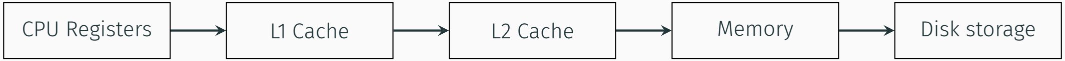
→ side effects on computations!

Memory Hierarchy



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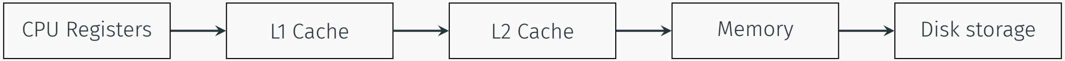

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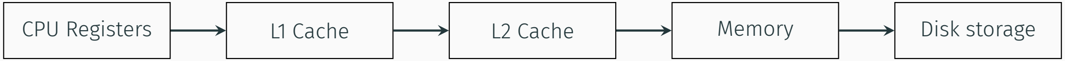

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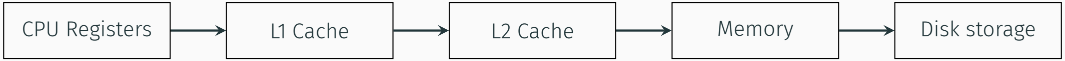

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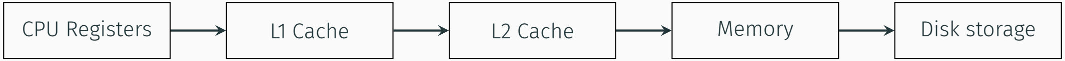
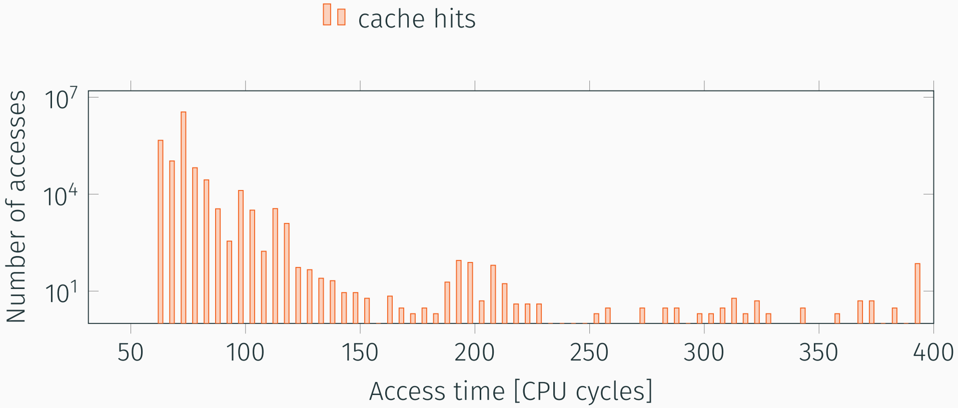


- Data can reside in
  - CPU registers
  - Different levels of the CPU cache
  - Main memory
  - Disk storage

Timing differences



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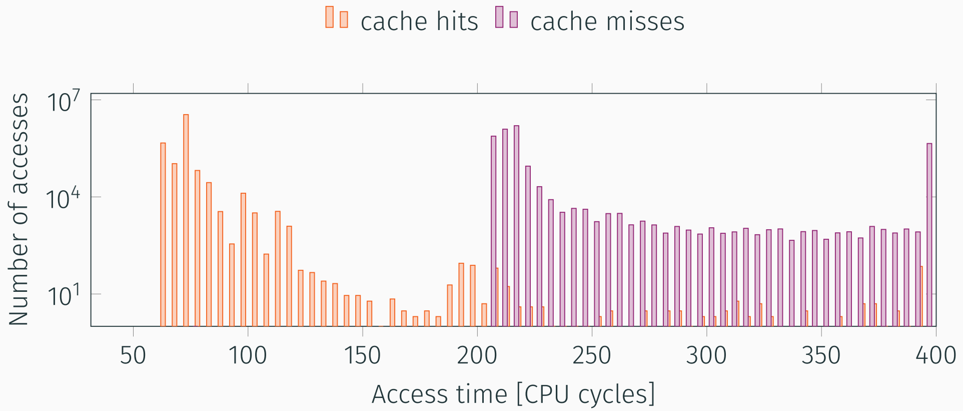

Cache attacks

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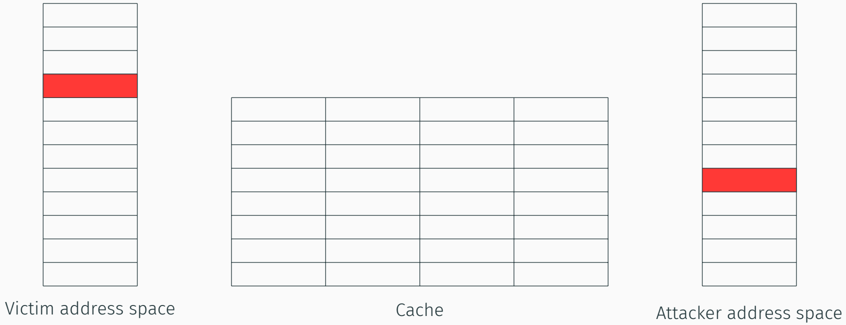
- cache attacks $\rightarrow$ exploit timing differences of memory accesses
- attacker monitors which lines are accessed, not the content
- covert channel: two processes communicating with each other
    - not allowed to do so, e.g., across VMs
- side-channel attack: one malicious process spies on benign processes
    - e.g., steals crypto keys, spies on keystrokes

Cache attacks: *Flush+Reload*



Step 1: Attacker maps shared library (shared memory, in cache)

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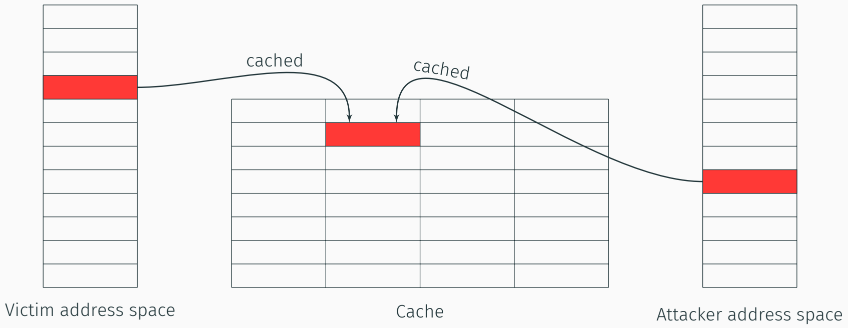

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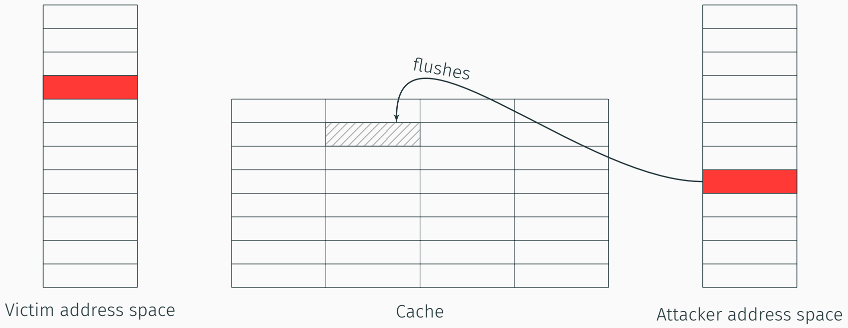

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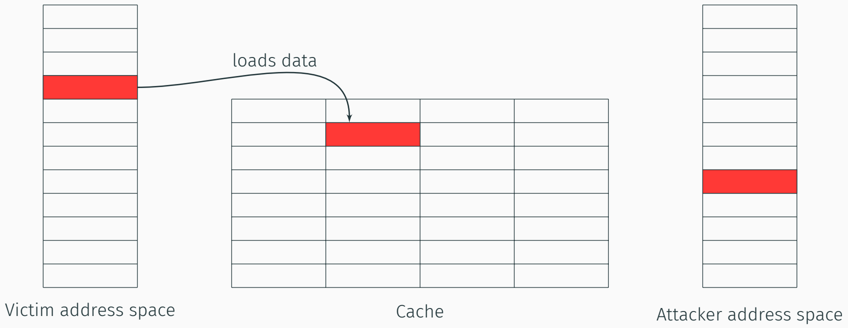

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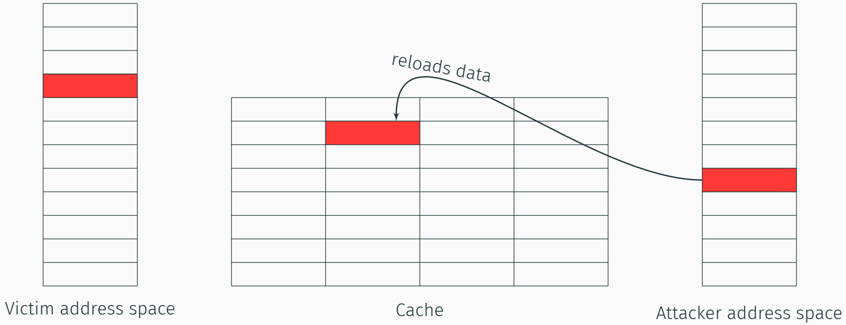

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Step 4: Attacker reloads the data

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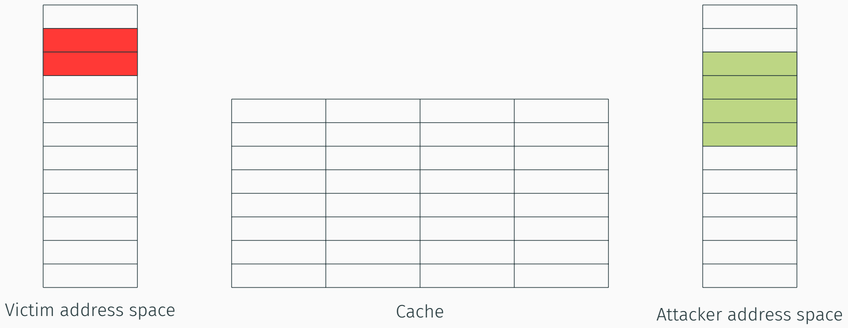

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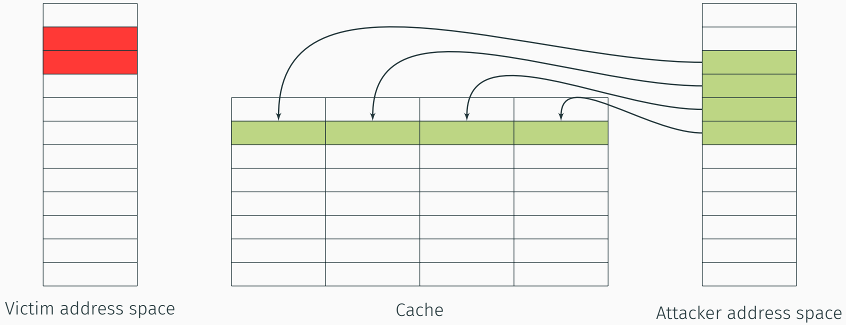

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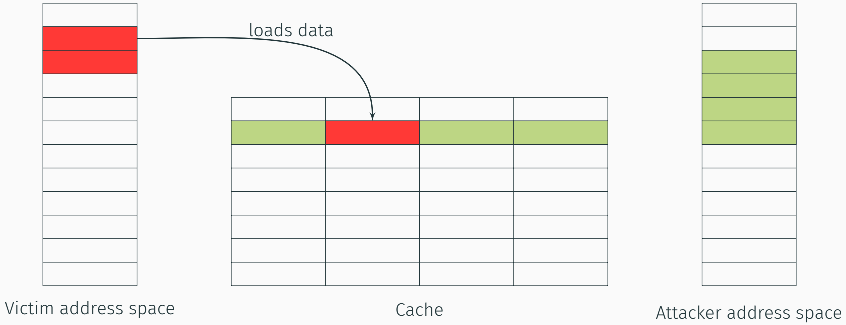

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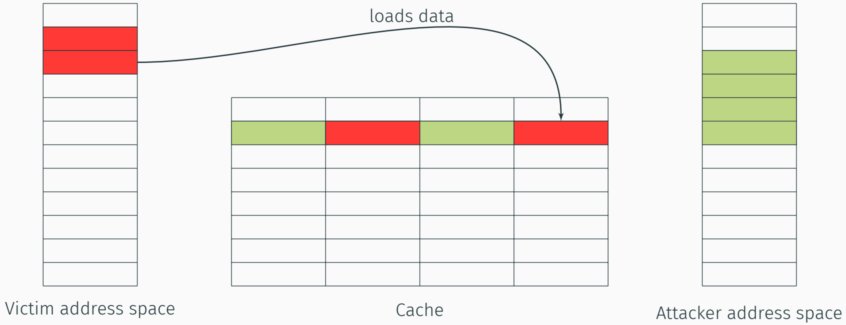

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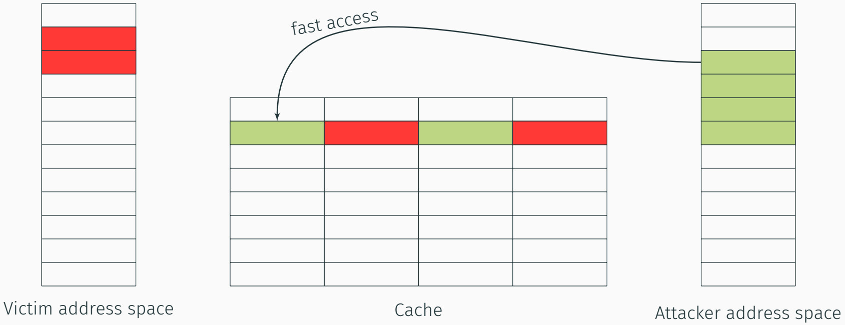

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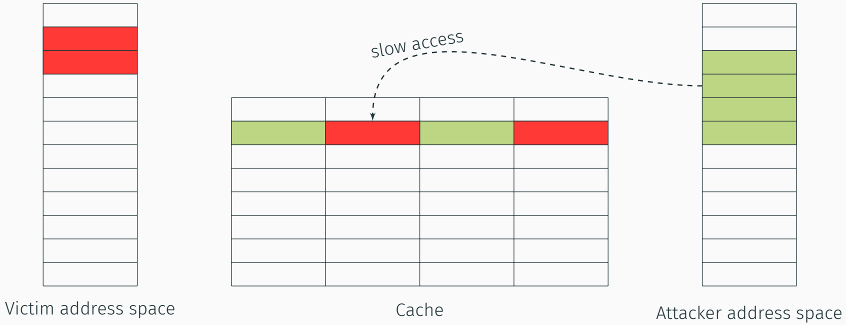

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Application #1

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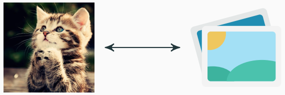

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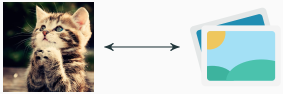

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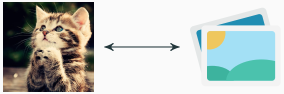

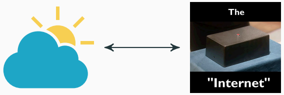

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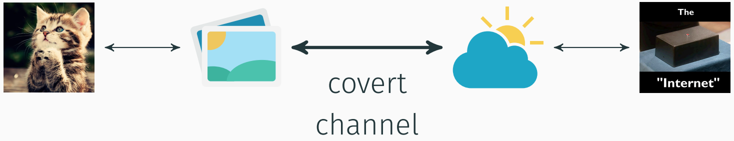

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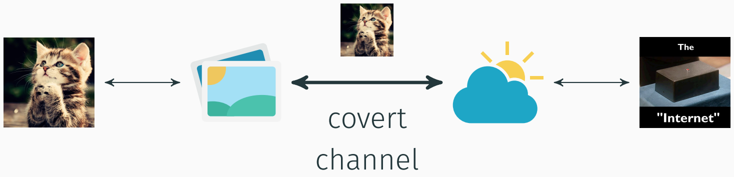

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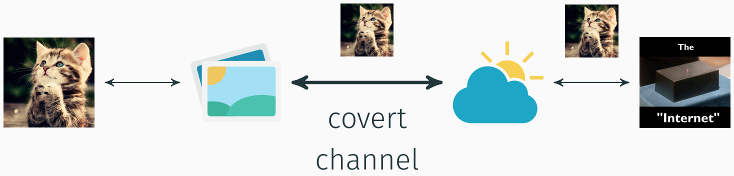

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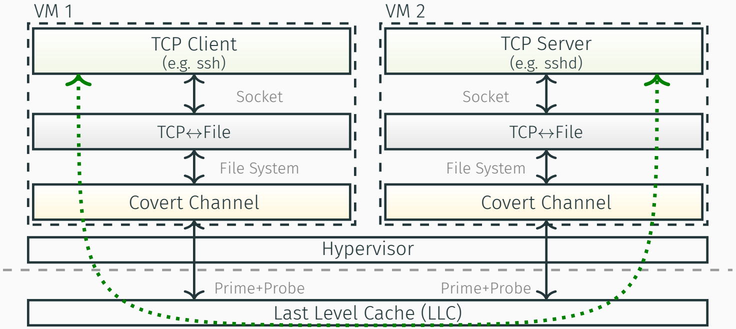
- sender and receiver agree on one set
- receiver probes the set continuously
- sender transmits ’0’ doing nothing
  - $\rightarrow$ lines of the receiver still in cache $\rightarrow$ fast access
- sender transmits ’1’ accessing addresses in the set
  - $\rightarrow$ evicts lines of the receiver $\rightarrow$ slow access

Application #1: Covert channel

- Prime+Probe: low requirements, works e.g., between VMs in Amazon EC2
  - error-free covert channel (40–75KBps) $\rightarrow$ SSH connection over the cache



C. Maurice, M. Weber, M. Schwarz, L. Giner, D. Gruss, C. A. Boano, S. Mangard, and K. Römer. "Hello from the Other Side: SSH over Robust Cache Covert Channels in the Cloud". In: *NDSS'17*. to appear. 2017.

Application #2

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- one-round known-plaintext attack by Osvik et al. (2006)
    - p plaintext and k secret key
    - intermediate state $x^{(r)} = (x_0^{(r)}, \dots, x_{15}^{(r)})$ at each round r
    - first round, accessed table indices are

$$x_i^{(0)} = p_i \oplus k_i \qquad \text{for all } i = 0, \dots, 15$$

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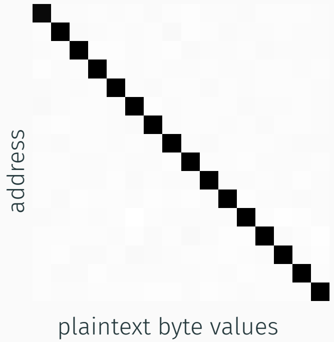
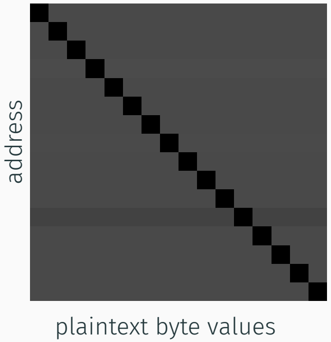
$\rightarrow$ recovering accessed table indices $\Rightarrow$ recovering the key

Application #2: Crypto side-channel attack

- monitoring which T-Table entry is accessed ($k_0 = \texttt{0x00}$)



Flush+Reload



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- it's an old attack...
- everything should be fixed by now...
- Bouncy Castle on Android $\rightarrow$ default implementation uses T-Tables
- many implementations you find online use pre-computed values

Application #3

Spying on keystrokes

Application #3: Spying on keystrokes

- Flush+Reload: fine-grained attack → spy on keystrokes

M. Lipp, D. Gruss, R. Spreitzer, C. Maurice, and S. Mangard. “ARMageddon: Cache Attacks on Mobile Devices”. In: *USENIX Security Symposium*. 2016

Application #3: Spying on keystrokes

- Flush+Reload: fine-grained attack → spy on keystrokes

Demo time!

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clflush

`clflush`—What could go wrong?

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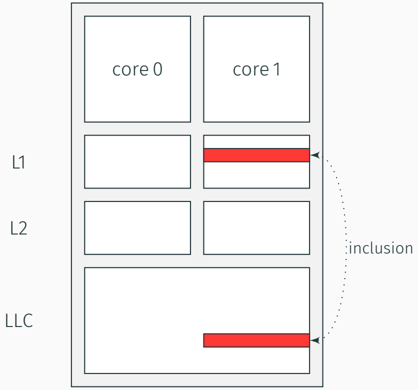
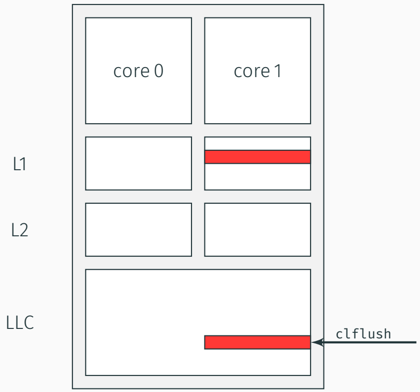
- `clflush`: invalidates from every level the cache line containing the address
- in itself enables Flush+Reload attacks
- but there's more!

`clflush` timing leakage: Part #1



- `clflush` on cached data

`clflush` timing leakage: Part #1



- `clflush` on cached data
    - goes to LLC, flushes line

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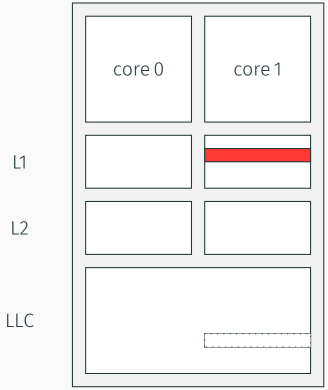

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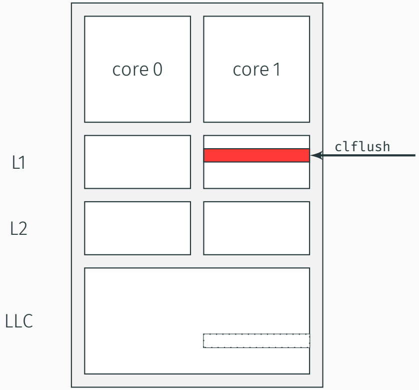

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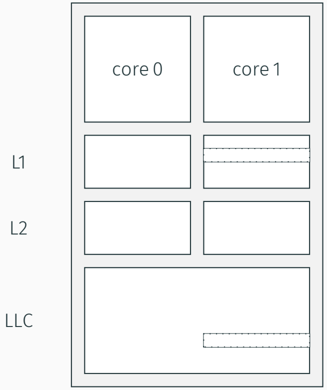

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  → slow

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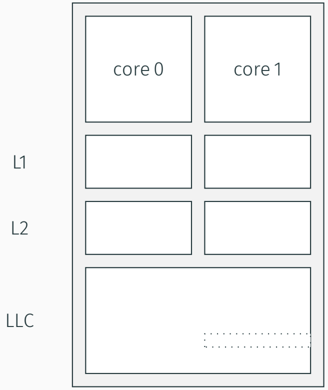

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- `clflush` on non-cached data

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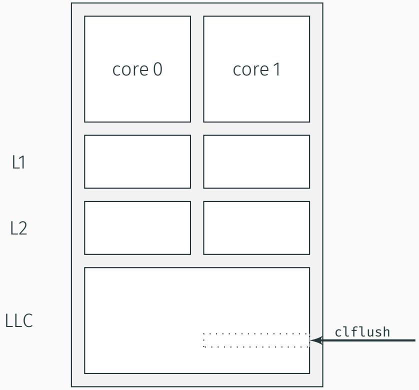

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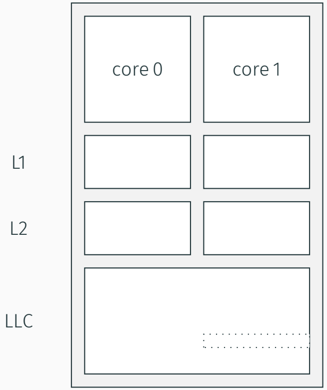

- `clflush` on cached data
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  → slow
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  - goes to LLC, does nothing

  → fast

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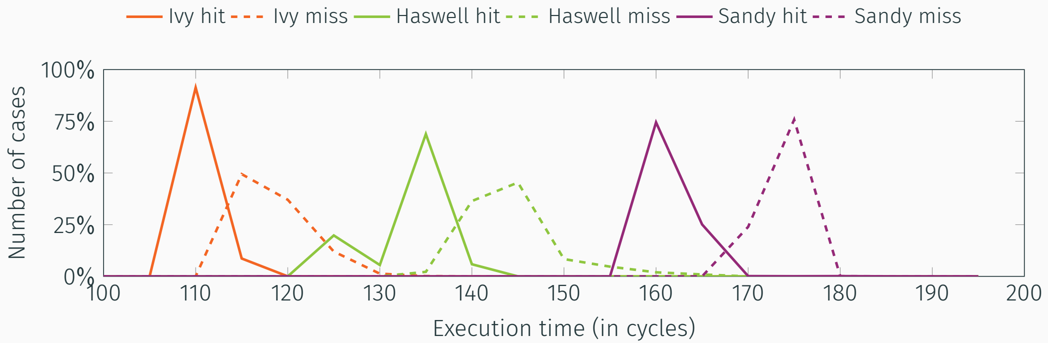

It’s only a few cycles, what could go wrong?!

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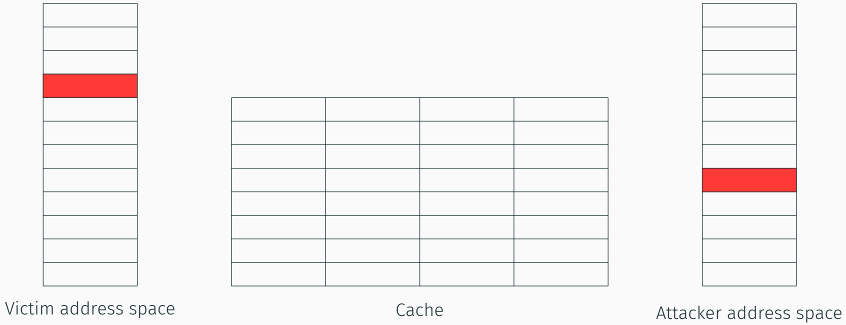

Step 1: Attacker maps shared library (shared memory, in cache)

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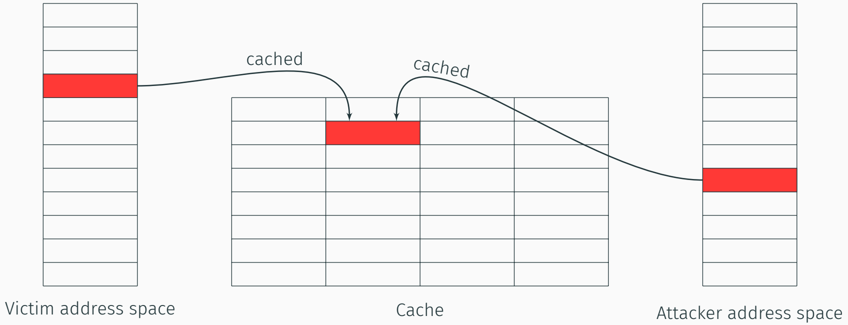

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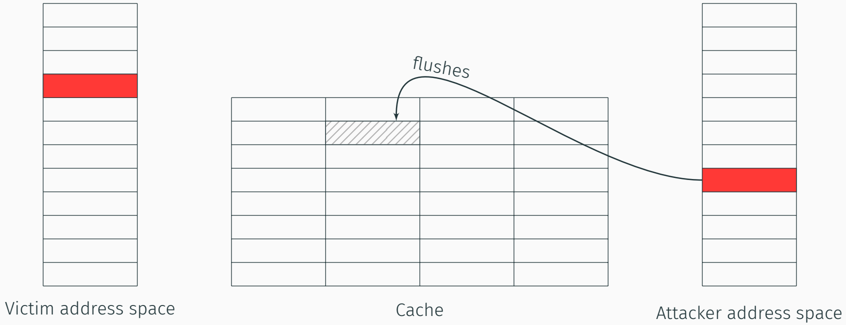

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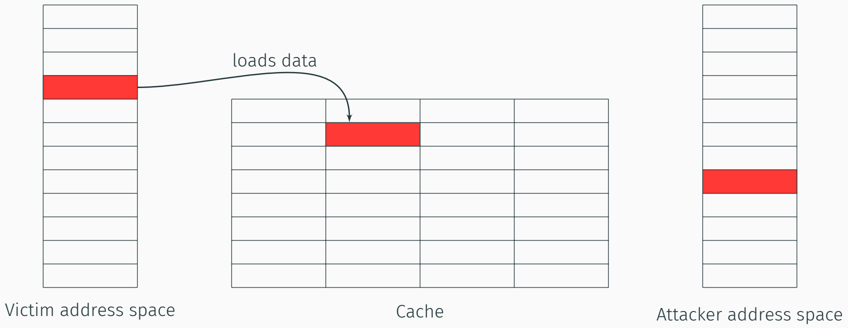

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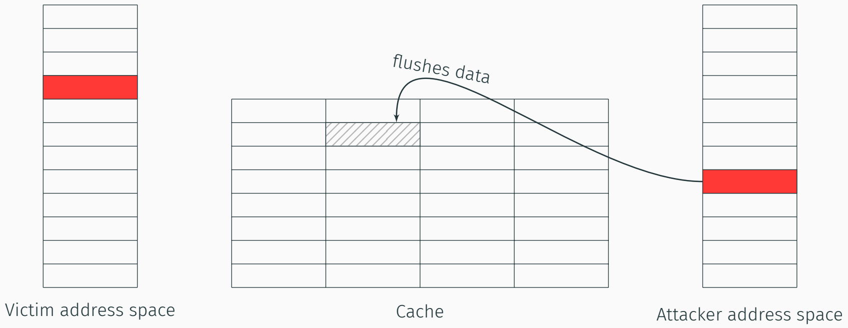

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Evaluating stealthiness

Detecting cache attacks and Rowhammer with performance counters

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$\rightarrow$ normalize the events by `ITLB_RA+ITLB_RM`

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Flush+Flush: Covert channel

technique	packet size	capacity (KBps)	receiver stealth	sender stealth
Flush+Flush	28			
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Flush+Flush: Covert channel

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Flush+Flush: Side channel on AES T-tables (1)

Number of encryptions to determine the upper 4 bits of a key byte

technique	number of encryptions
Flush+Reload	250
Flush+Flush	350
Prime+Probe	4 800

$\rightarrow$ same performance for Flush+Flush and Flush+Reload

Flush+Flush: Side channel on AES T-tables (2)

Stealthiness comparison on 256 million encryptions (synchronous attack)

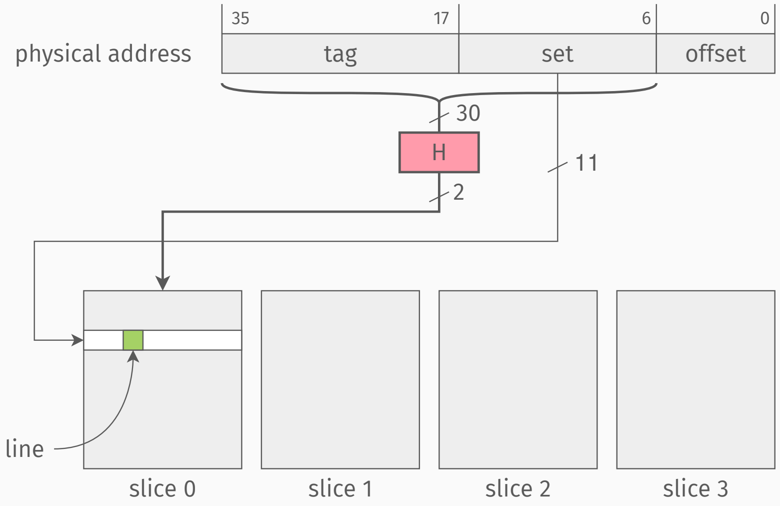
technique	time (s)	stealth
Flush+Reload	215	✗
Prime+Probe	234	✗
Flush+Flush	163	✓

→ Flush+Flush is the only stealth spy process

→ others need to be slowed down too much to be practical

A little bit more background before continuing…

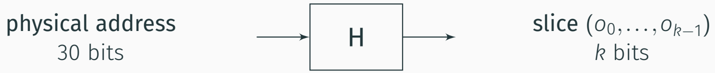
Last-level cache (1)



Last-level cache (2)

- last-level cache $\rightarrow$ as many slices as cores
- undocumented hash function that maps a physical address to a slice
- designed for performance

For 2^k slices:



Let’s go back to `clflush`!

`clflush` timing leakage: Part #2

- `clflush` faster to reach a line on the local slice

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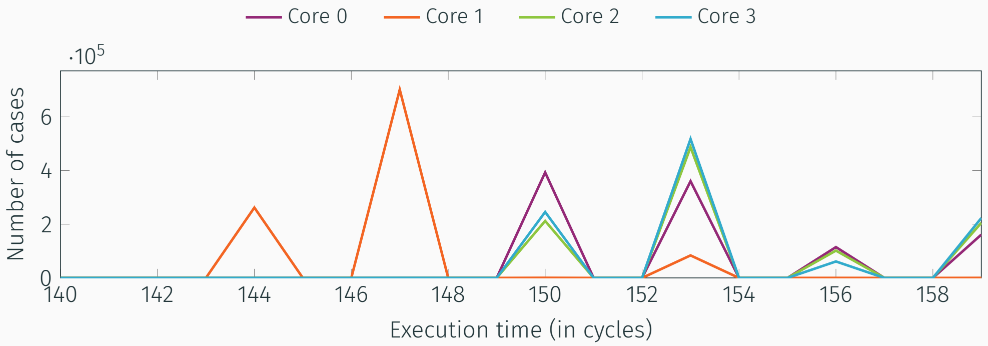

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- one way to reverse-engineer the addressing function

`clflush` timing leakage: Part #2

- map physical addresses to slices
- one way to reverse-engineer the addressing function
- other way: using performance counters[1]

[1] C. Maurice, N. Le Scouarnec, C. Neumann, O. Heen, and A. Francillon. “Reverse Engineering Intel Complex Addressing Using Performance Counters”. In: *RAID'15*. 2015

prefetch

`prefetch` instructions

`prefetch` fetches the line of data from memory containing the specified byte

6 `prefetch` instructions:

- `prefetcht0`: suggests CPU to load data into L1
- `prefetcht1`: suggests CPU to load data into L2
- `prefetcht2`: suggests CPU to load data into L3
- `prefetchnta`: suggests CPU to load data for non-temporal access
- `prefetchw`: suggests CPU to load data with intention to write
- `prefetchwt1`: suggests CPU to load vector data with intention to write

`prefetch` according to Intel

NOTE

Intel Corporation. *Intel® 64 and IA-32 Architectures Optimization Reference Manual.* 2014

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Using the PREFETCH instruction is recommended only if data does not fit in cache.

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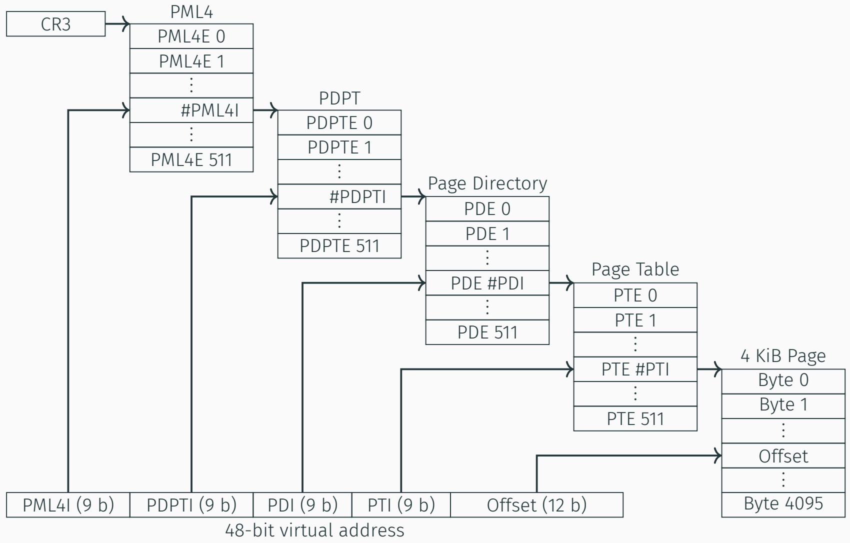
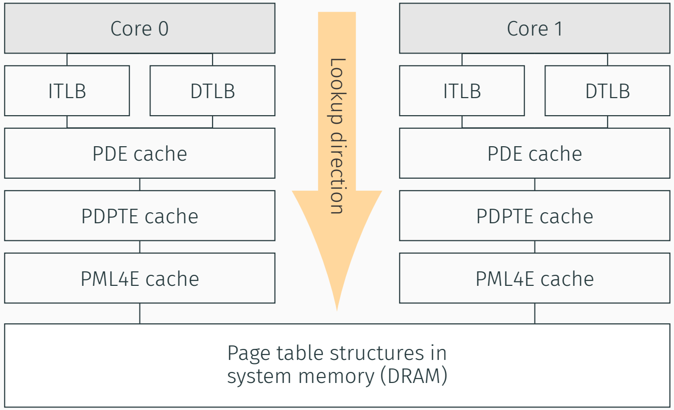
A little bit more background before continuing...

Address translation

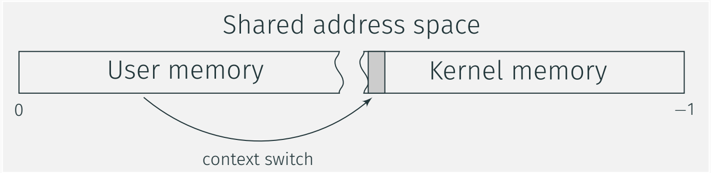


Address translation caches

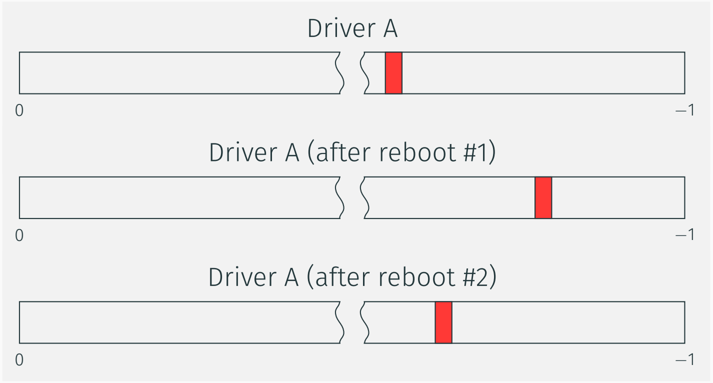


Kernel is mapped in every process

Today’s operating systems:



Kernel Address Space Layout Randomization (KASLR)



- same driver, different offset at each boot

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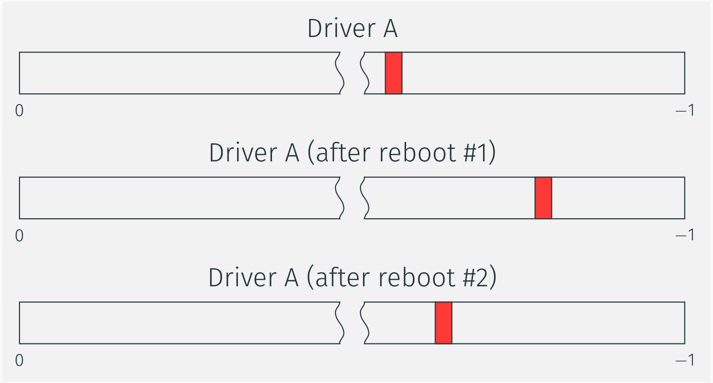
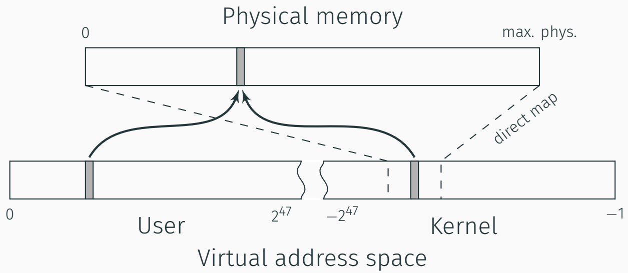


- same driver, different offset at each boot
- leaking kernel/driver addresses defeats KASLR

Kernel direct-physical map



- OS X, Linux, BSD, Xen PVM (Amazon EC2)

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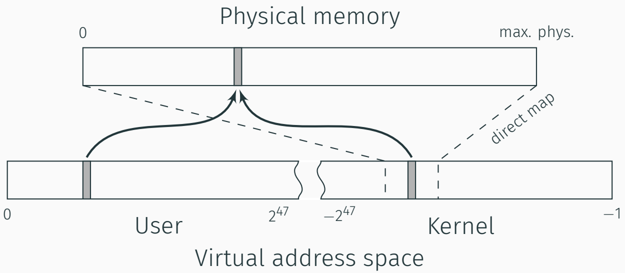

- OS X, Linux, BSD, Xen PVM (Amazon EC2)
- not Windows

Let’s go back to `prefetch`!

`prefetch`: Unusual instructions (1)

- tells the CPU “I might need that later”

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Property #1: do not check privileges

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`prefetch`: Unusual instructions (2)

- operand is a virtual address

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Property #2: execution time varies

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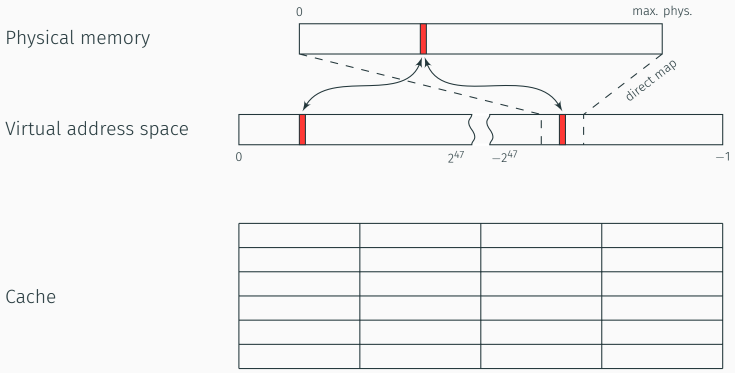
Address-translation oracle

Exploiting property #1 + kernel direct-physical map



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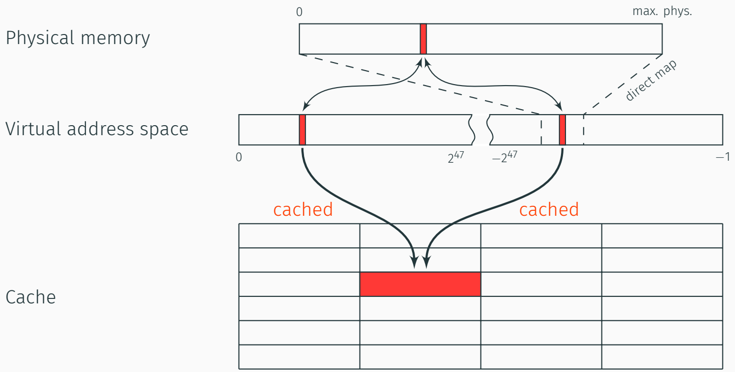

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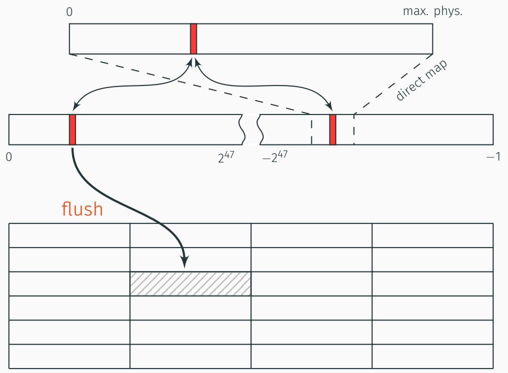

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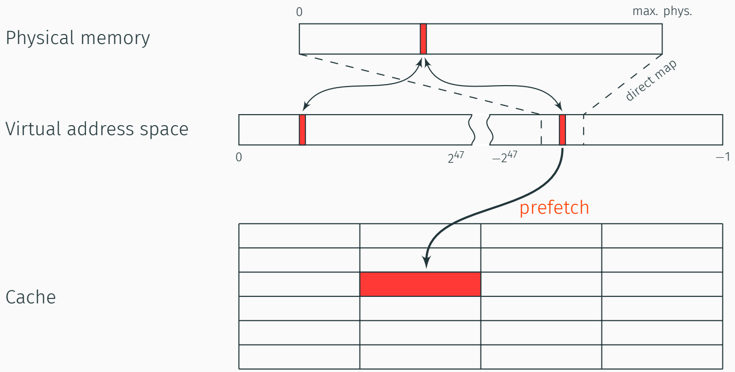

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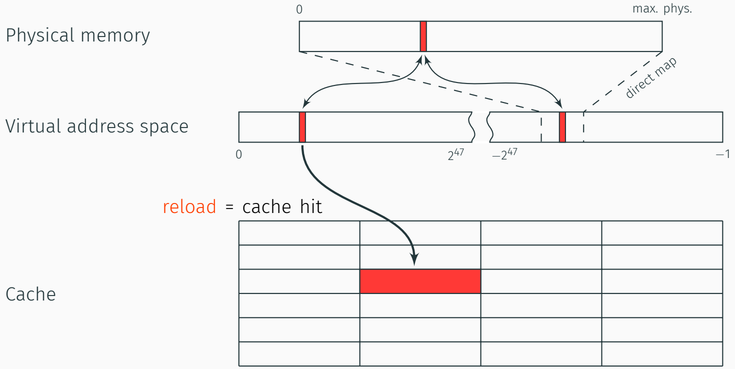
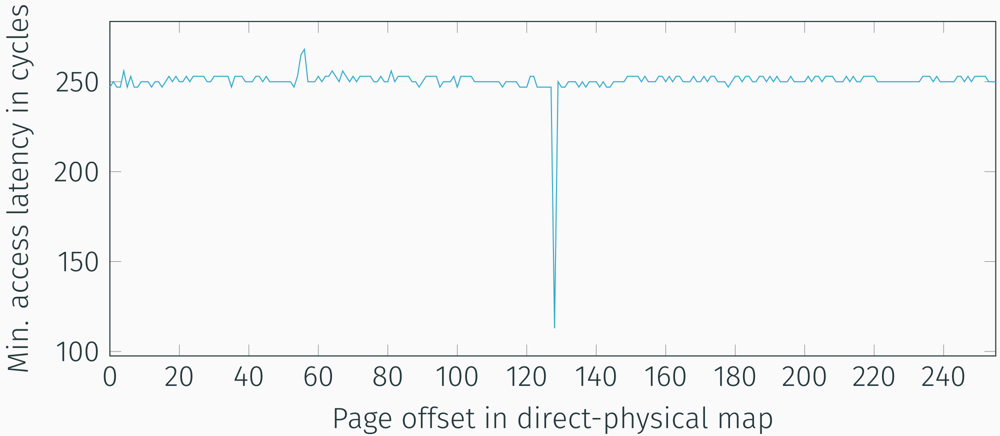


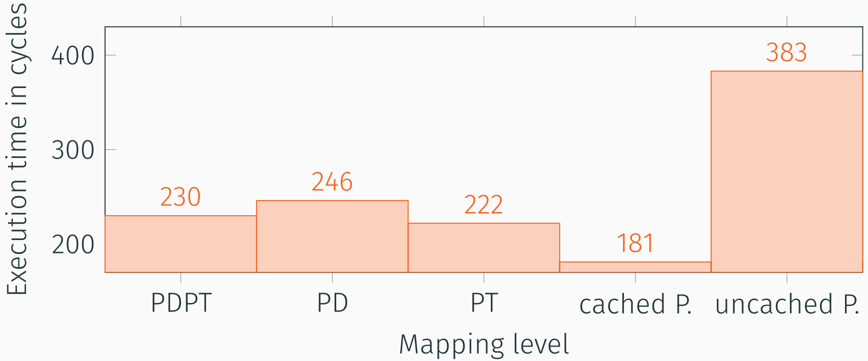
- cache hit → physical address in kernel mapping is the correct translation

Address-translation oracle



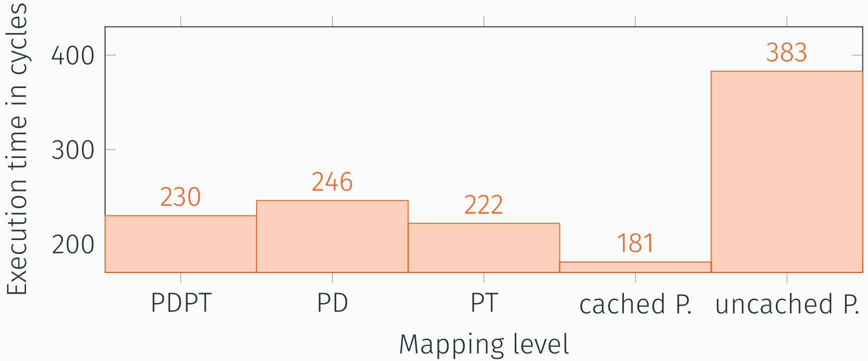
Translation-level oracle

Exploiting property #2



Translation-level oracle

Exploiting property #2



- timing depends on where the translation stops

Prefetch side-channel attacks

Using the two oracles

Prefetch side-channel attacks

Using the two oracles

- variants of cache attacks (e.g., Flush+Prefetch)

Prefetch side-channel attacks

Using the two oracles

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- translating virtual addresses to physical addresses (→ `/proc/pid/pagemap`)
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- locating kernel drivers
  - → bypasses KASLR

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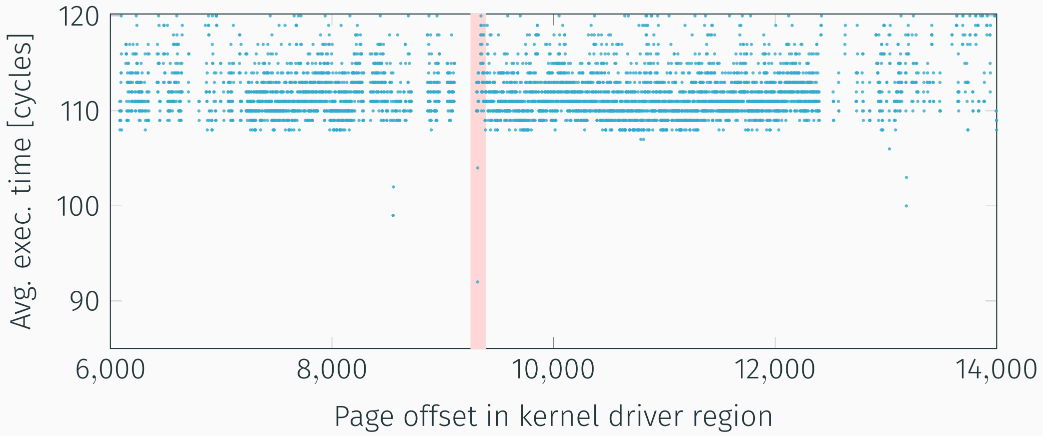
Full attack on Windows 10 in $<$ 12 seconds

Defeating KASLR by locating kernel driver (2)



That’s not all folks!

`rdseed` and floating point operations

- `rdseed`
  - request a random seed to the hardware random number generator
  - fixed number of precomputed random bits, takes time to regenerate them

  $\rightarrow$ covert channel

D. Evtyushkin and D. Ponomarev. “Covert Channels through Random Number Generator: Mechanisms, Capacity Estimation and Mitigations”. In: *CCS'16*. 2016

M. Andrysco, D. Kohlbrenner, K. Mowery, R. Jhala, S. Lerner, and H. Shacham. “On subnormal floating point and abnormal timing”. In: *S&P'15*. 2015

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- `fadd`, `fmul`
  - floating point operations
  - running time depends on the operands

  → bypassing Firefox's same origin policy via SVG filter timing attack

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`jmp` and TSX instructions

- `jmp`
  - branch prediction and branch target prediction
  - → covert channels, side-channel attacks on crypto, bypassing kernel ASLR

O. Acıiçmez, J.-P. Seifert, and c. K. Koç. “Predicting secret keys via branch prediction”. In: *CT-RSA 2007*. 2007

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`jmp` and TSX instructions

- `jmp`
  - branch prediction and branch target prediction

  → covert channels, side-channel attacks on crypto, bypassing kernel ASLR
- TSX instructions
  - extension for hardware transactional memory support

  → bypassing kernel ASLR

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- hard to patch → issues linked to performance optimizations
- quick fixes like removing instructions won't work

→ we keep finding new instructions that leak information

What could possibly go wrong with <insert x86 instruction here>?

Clémentine Maurice, Moritz Lipp

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