

A 10GE Monitoring System

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ariën@ams-ix.net

Agenda

- Introduction

The role of an internet exchange (IX).

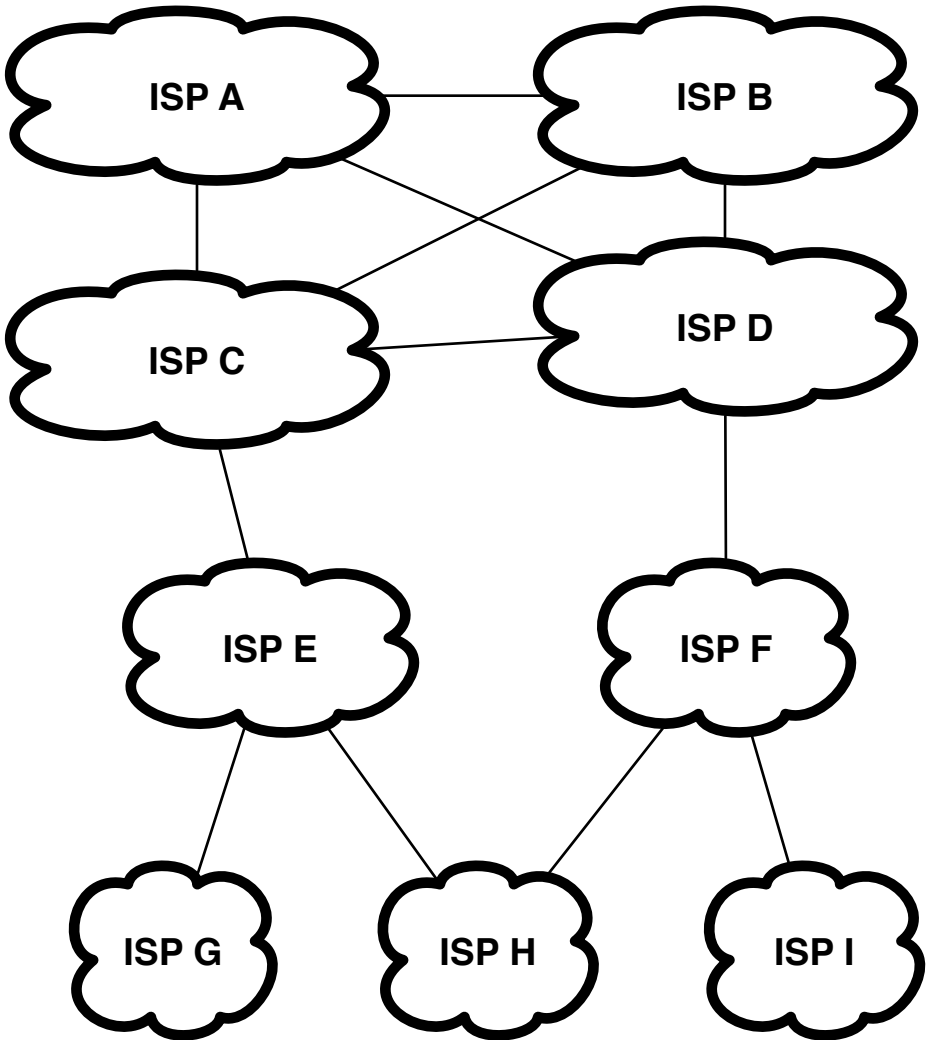
- The problem to be solved.

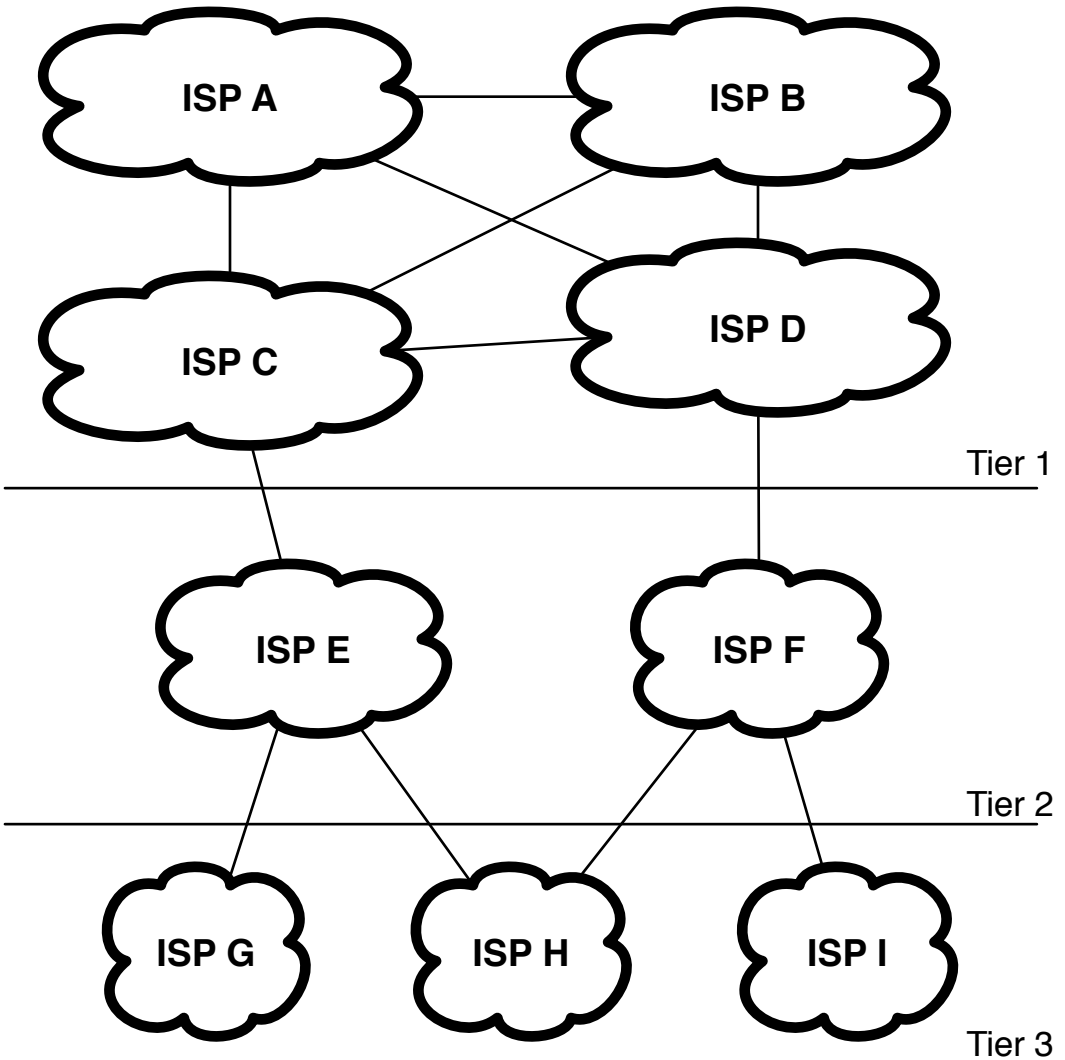
Real life examples

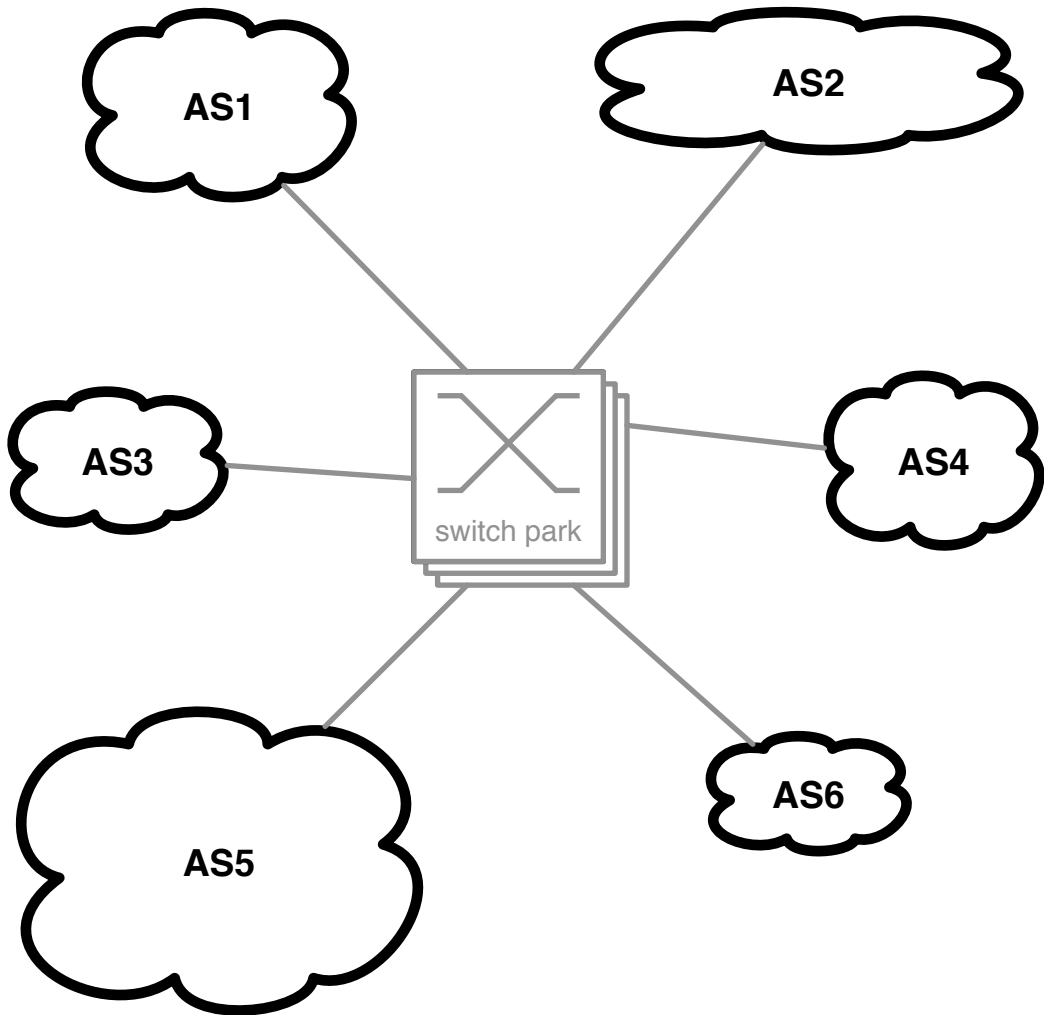
- The chosen solution for that problem

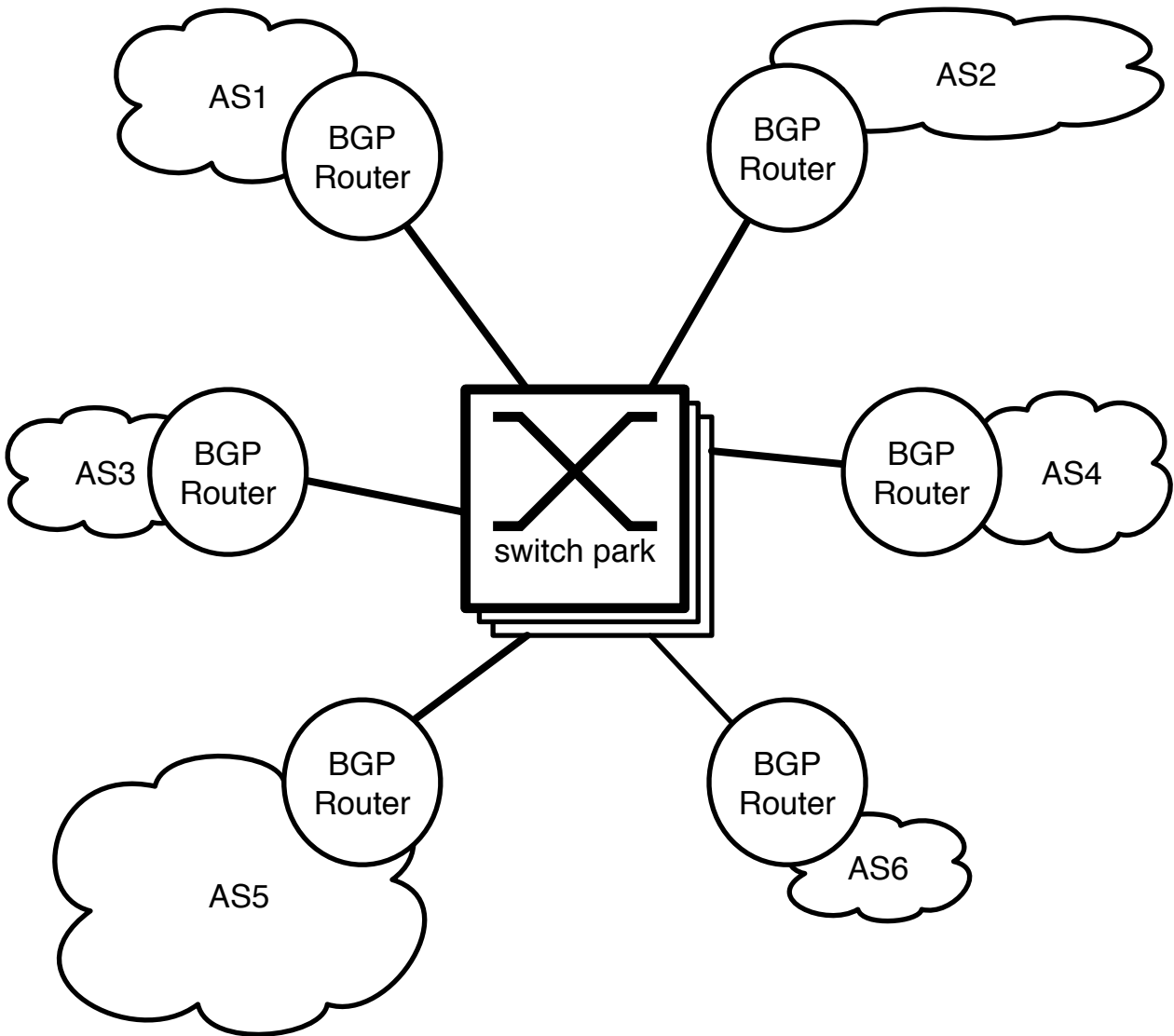
- * The Force10's P10 IDS/IPS card

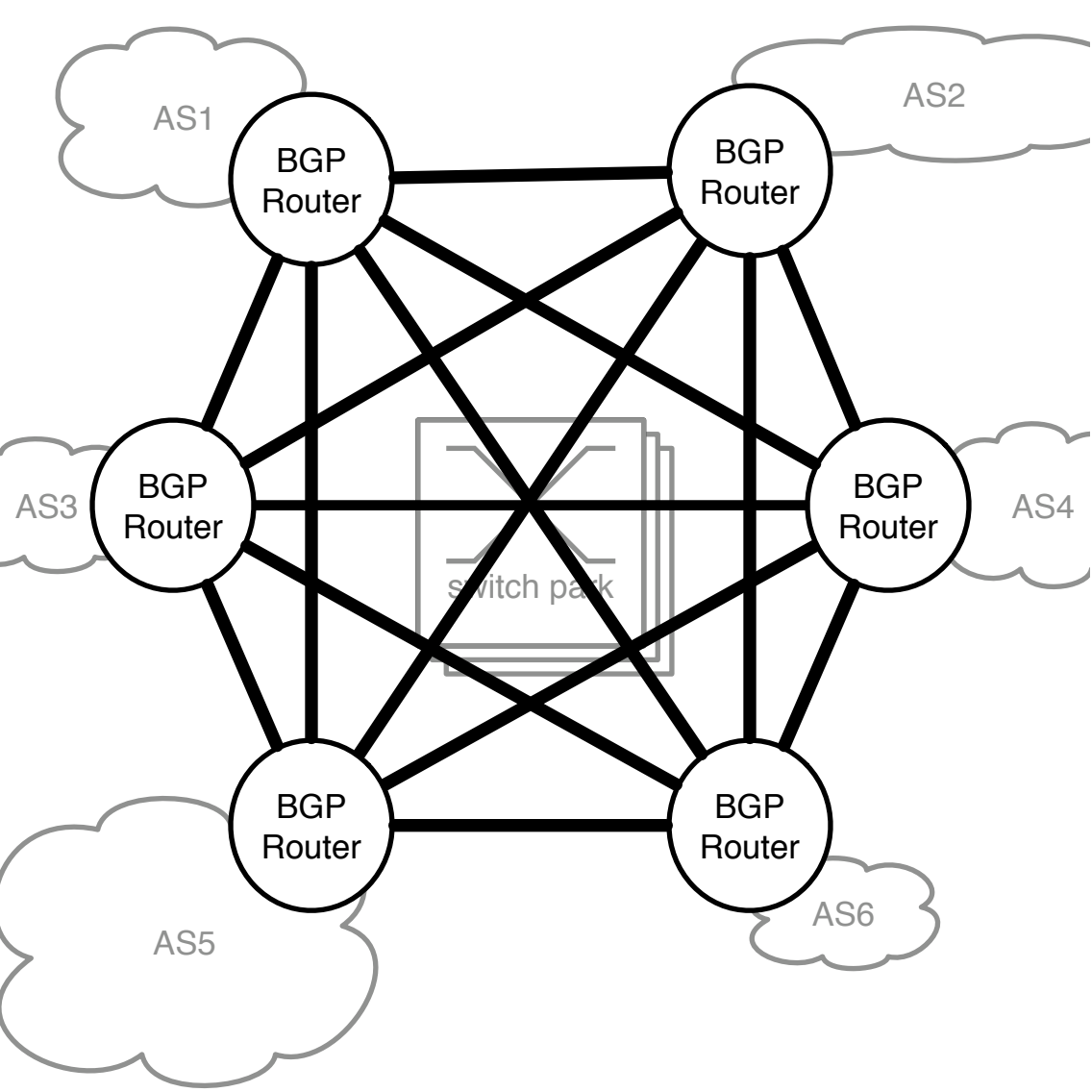
- * Photonic cross connects

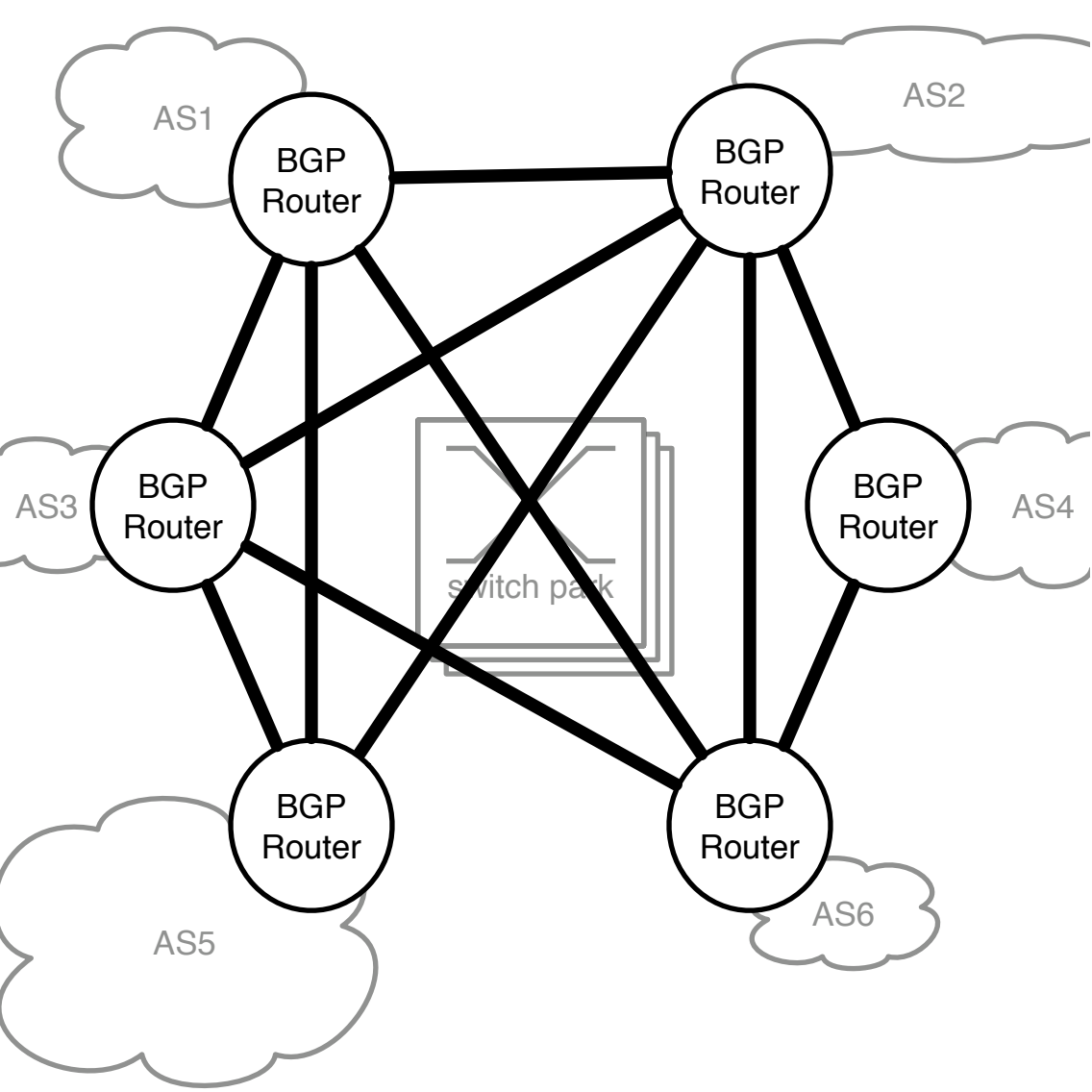


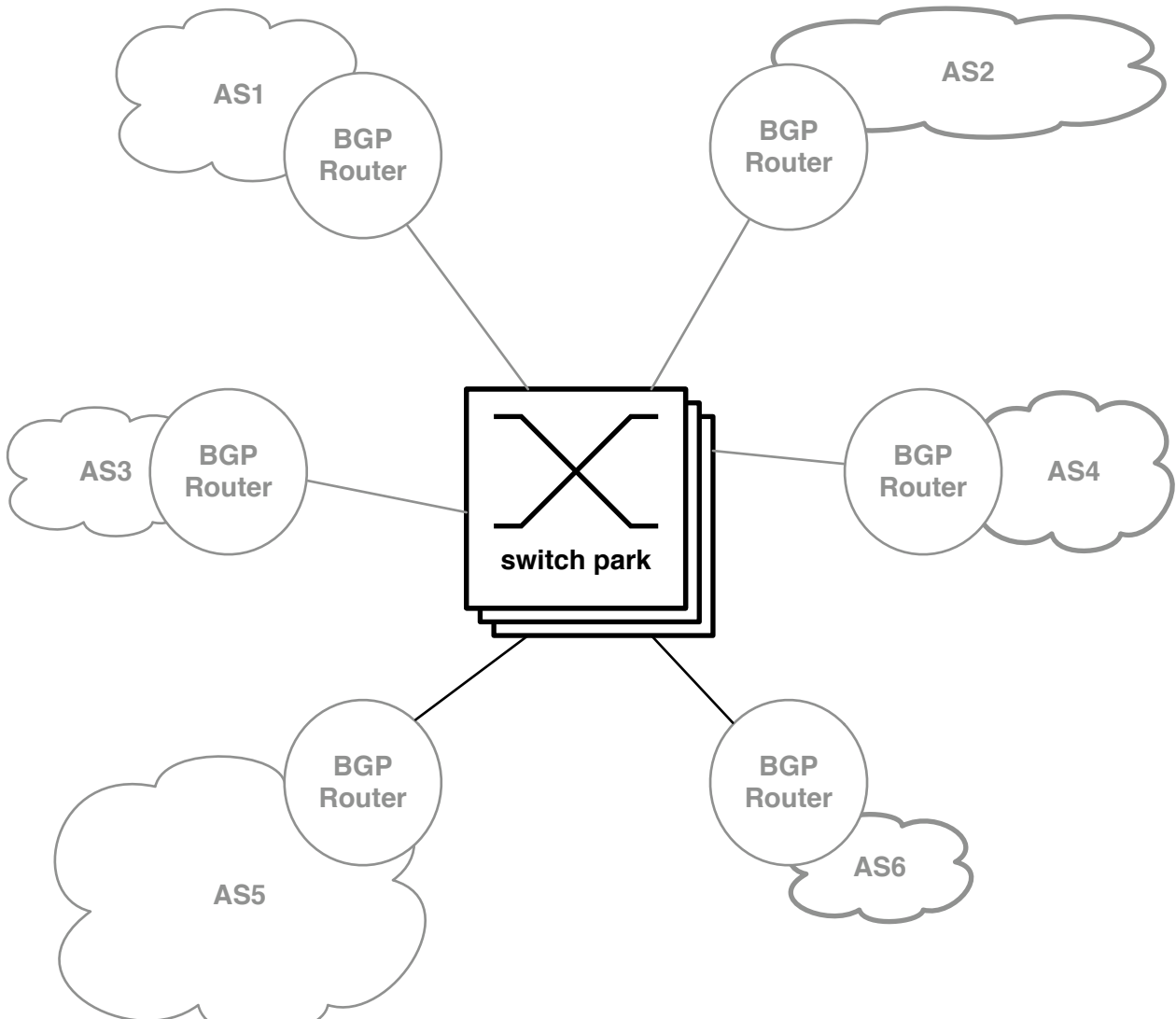


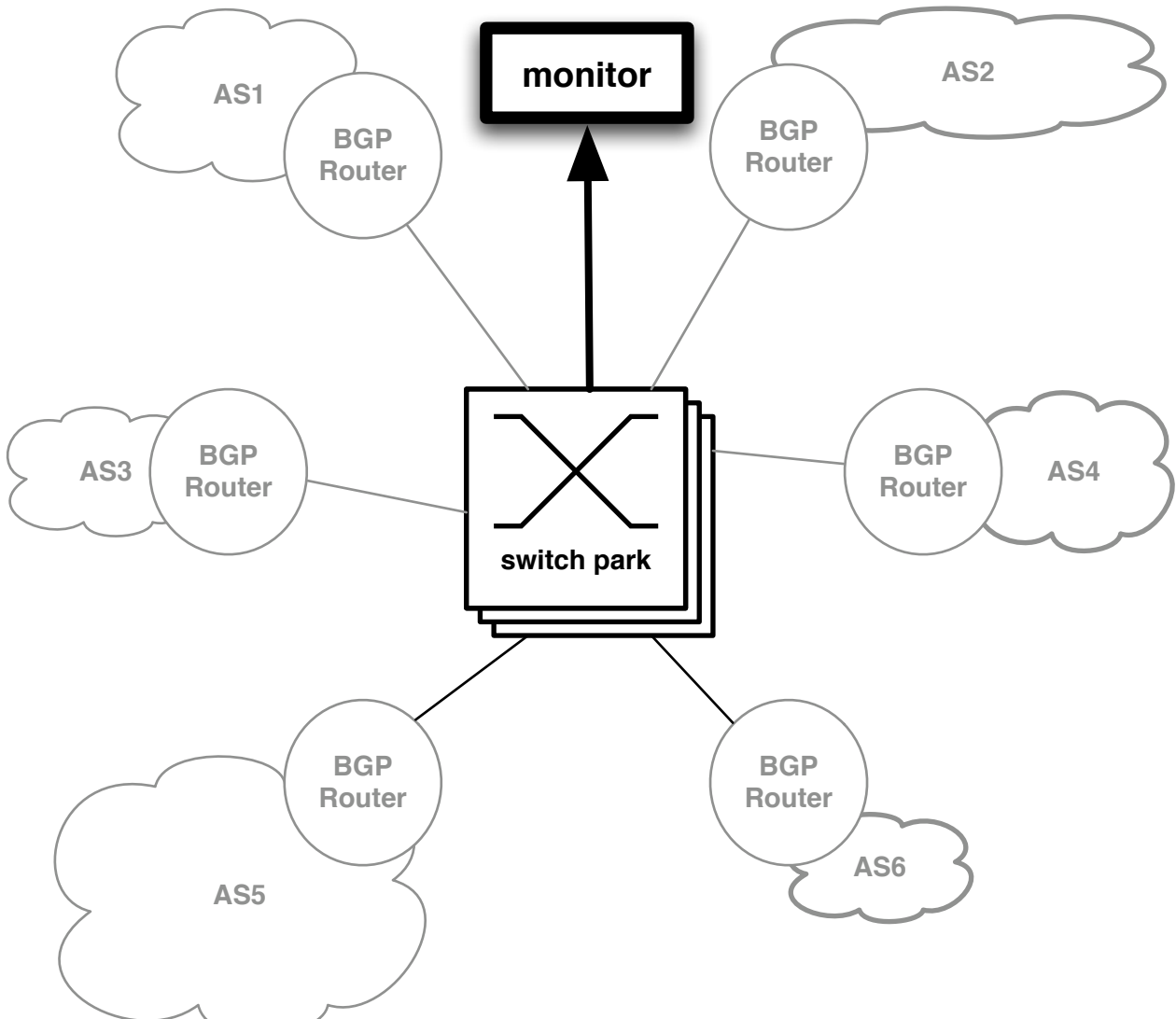




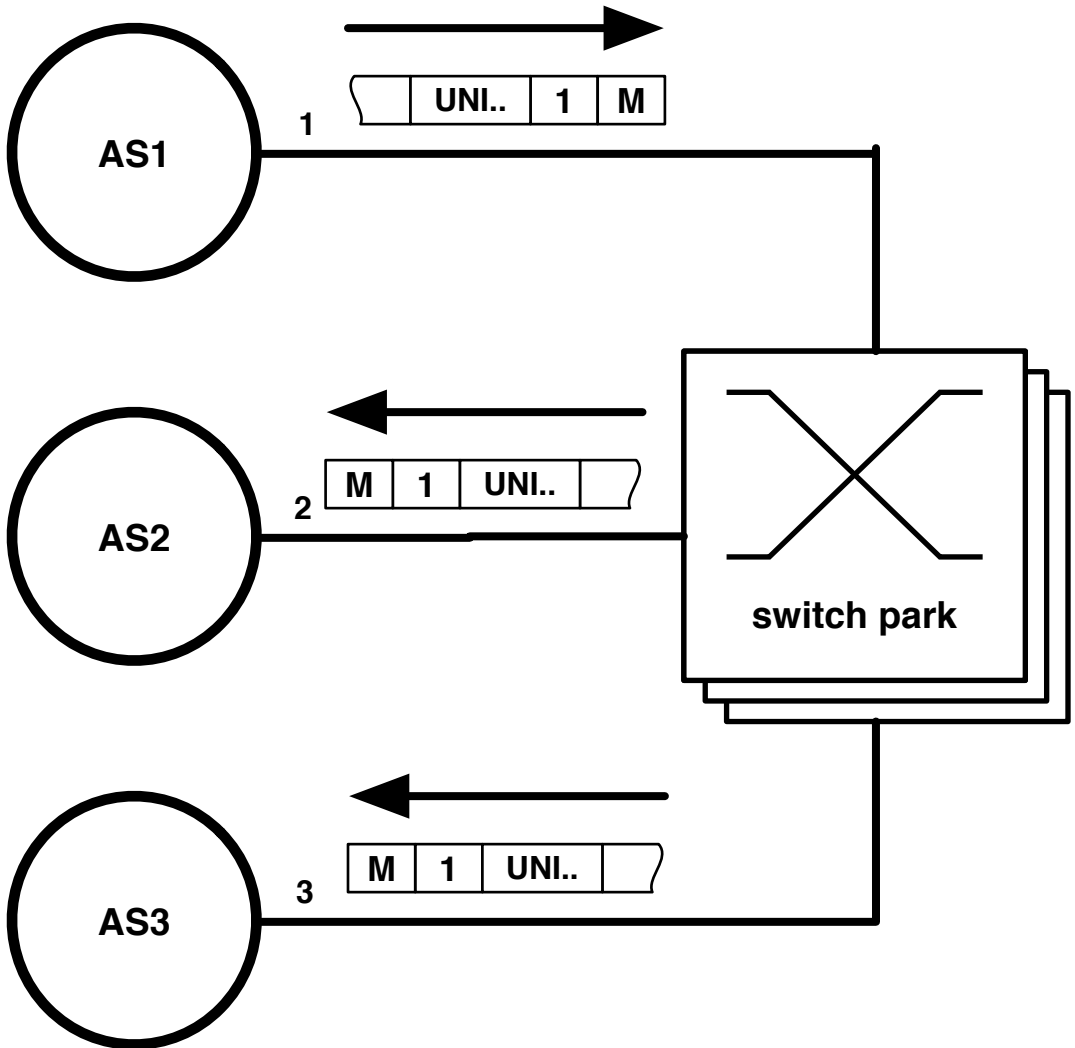


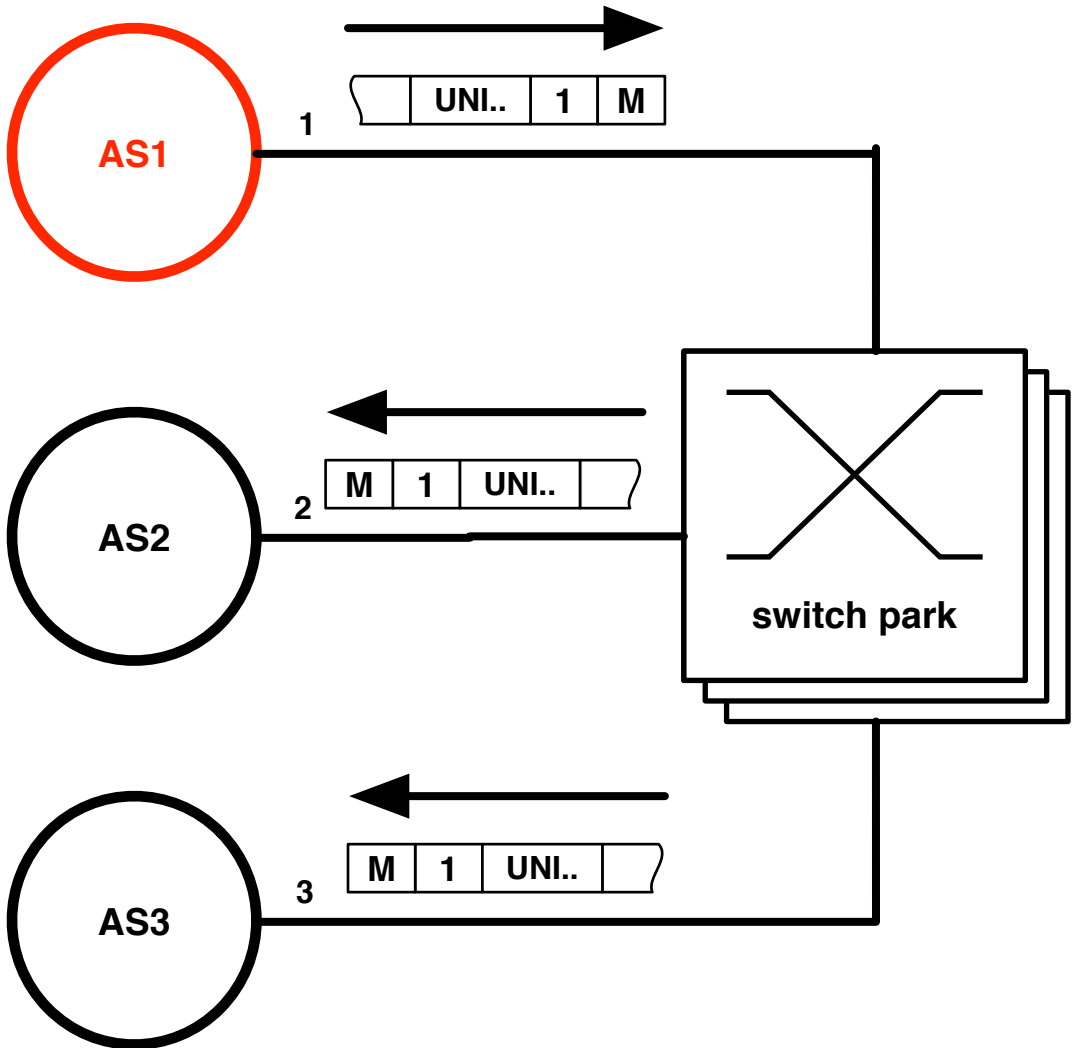


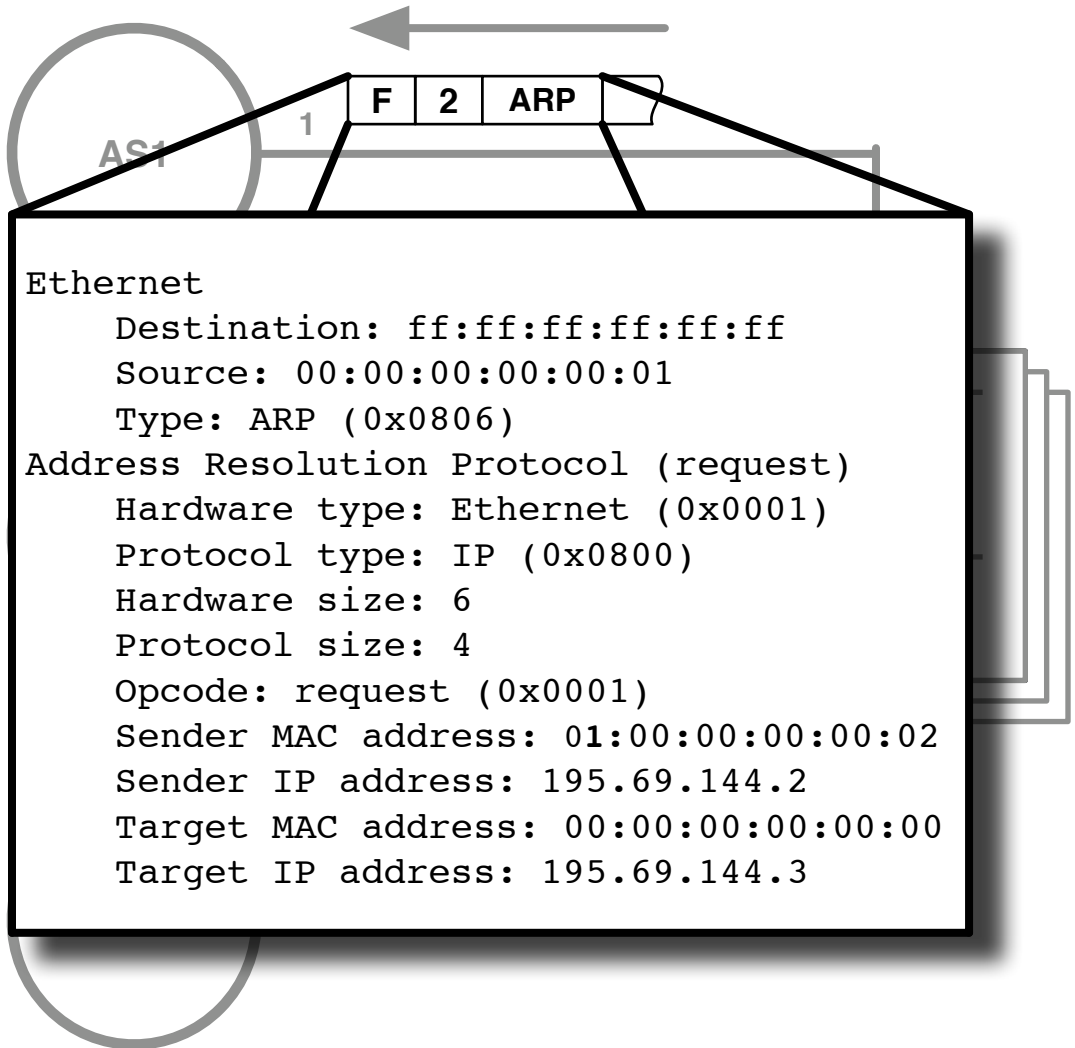


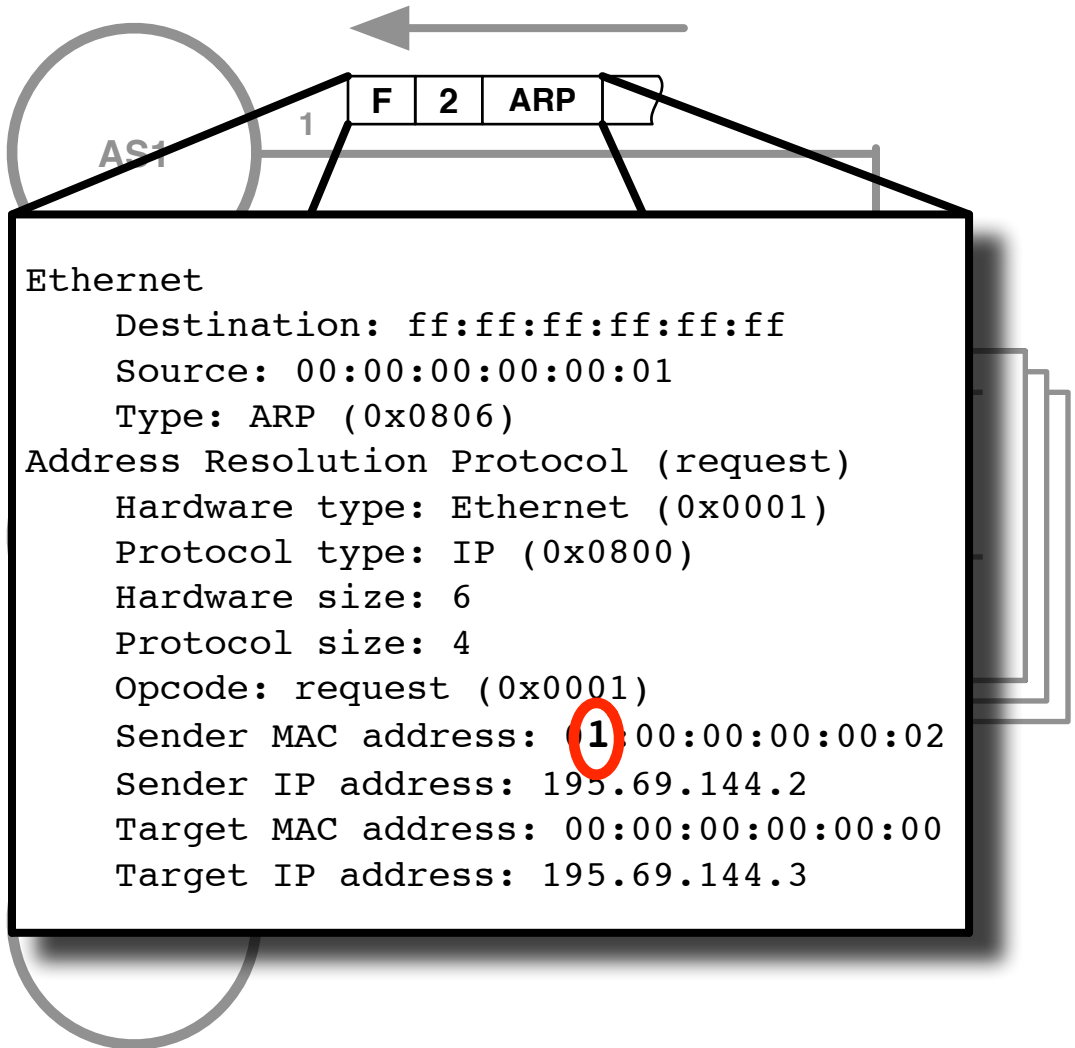


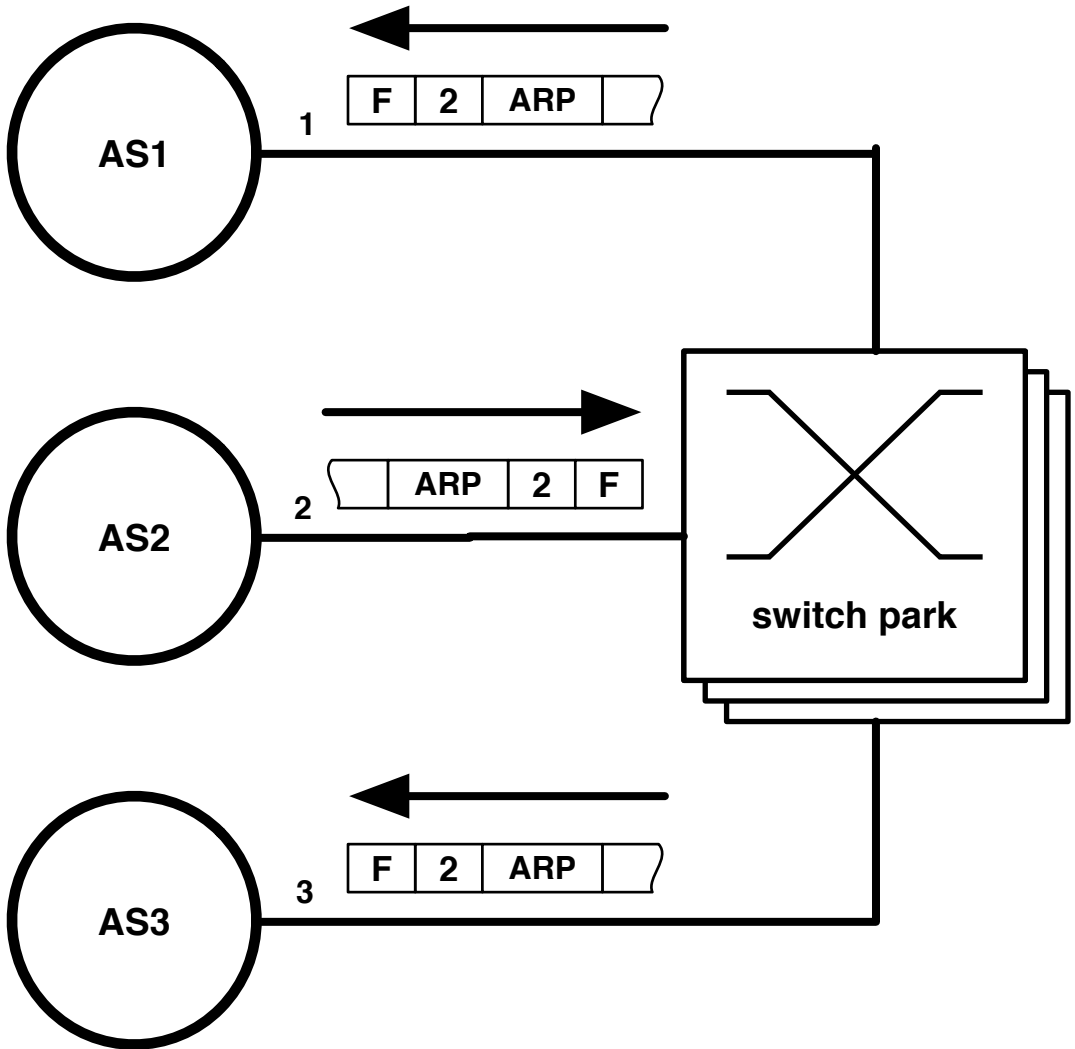
Example #1



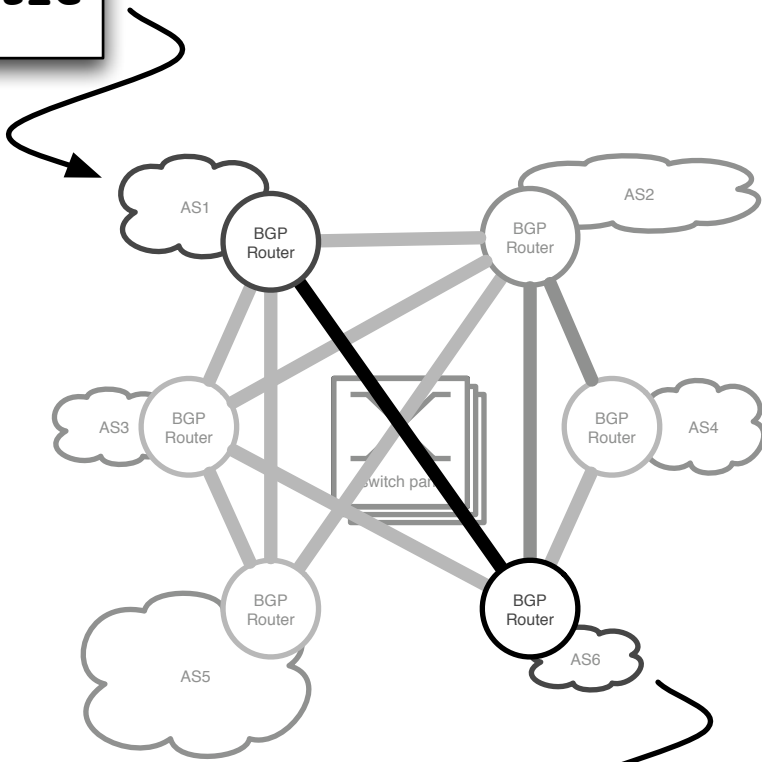






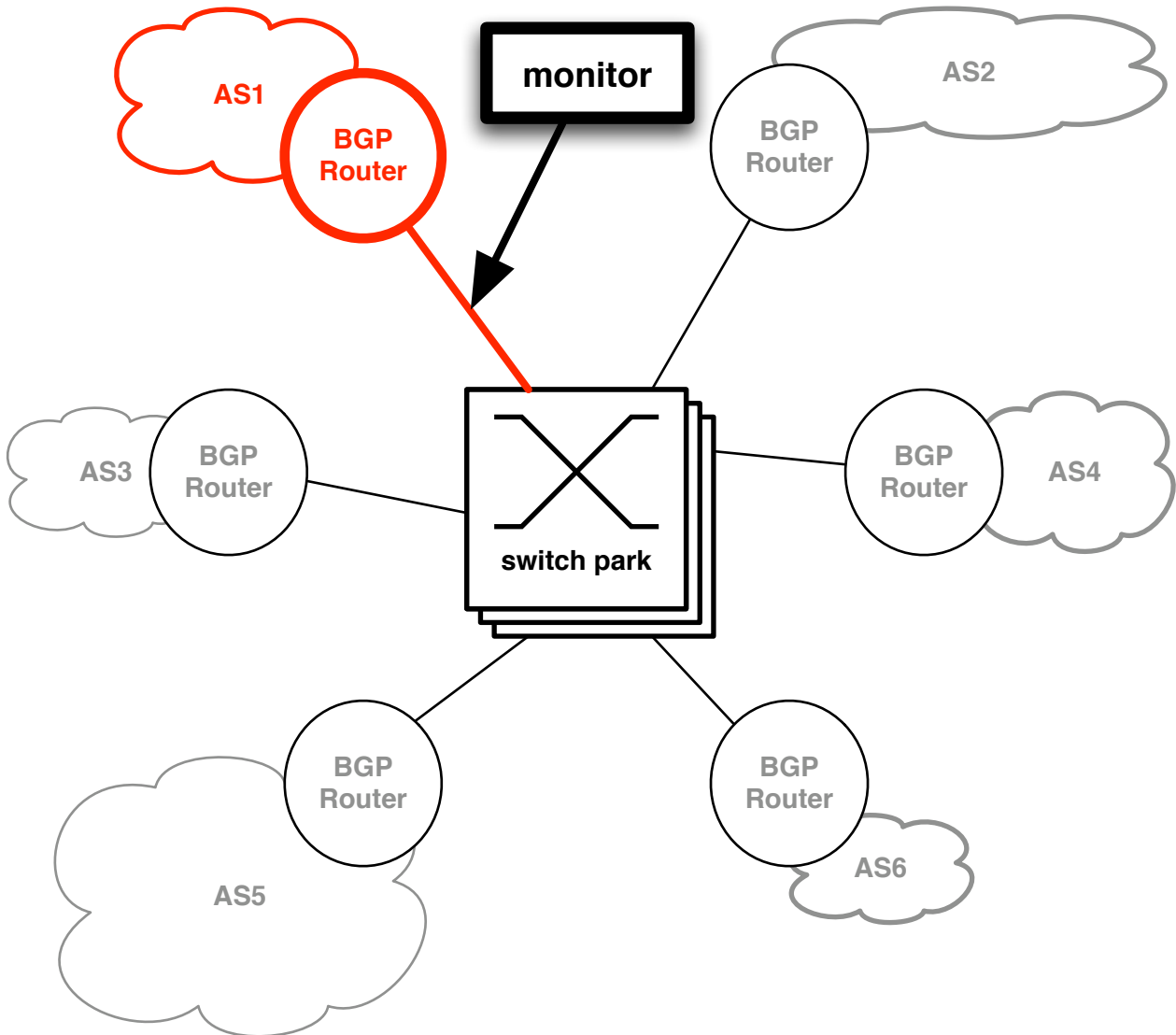


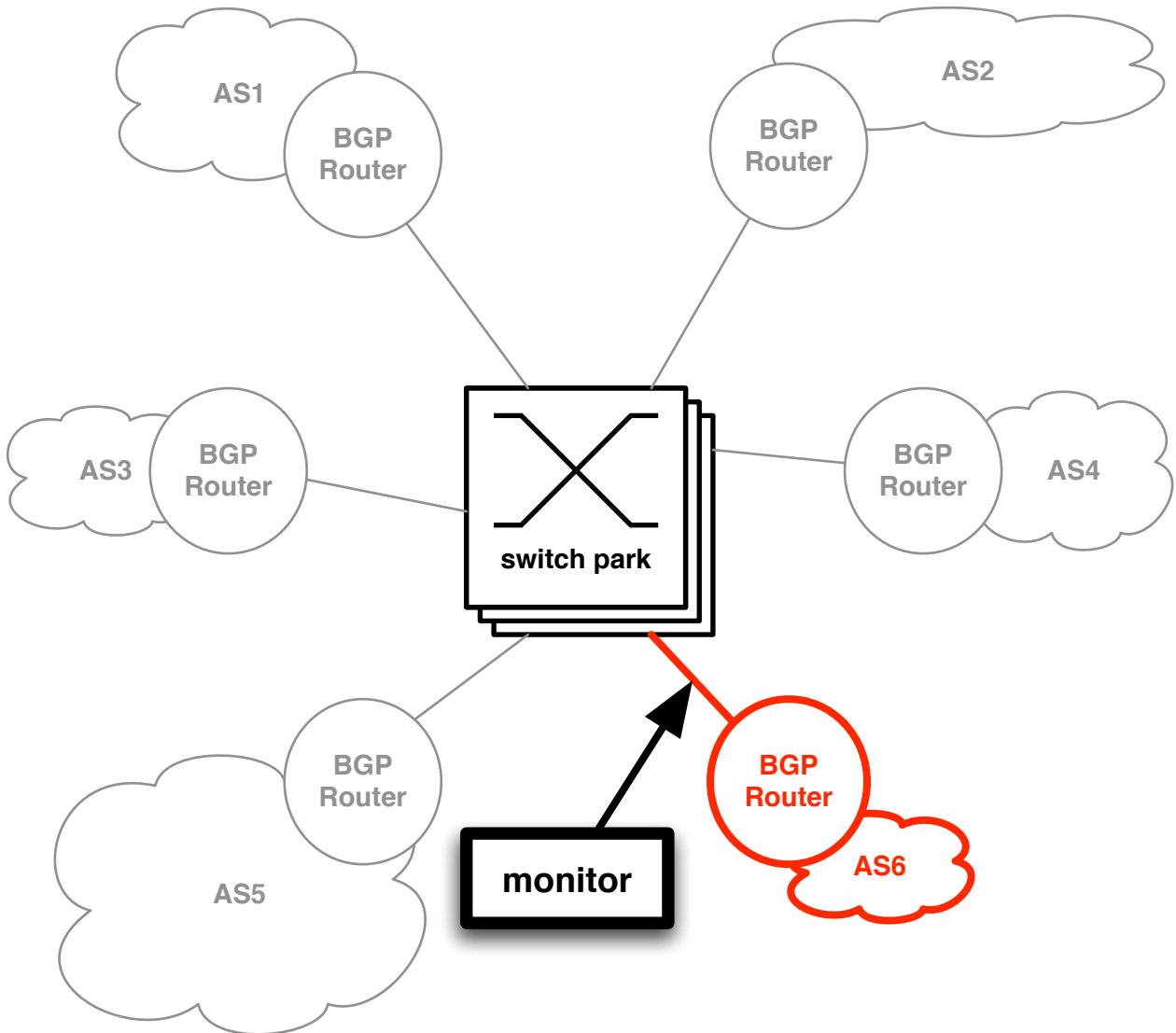
Tuttle

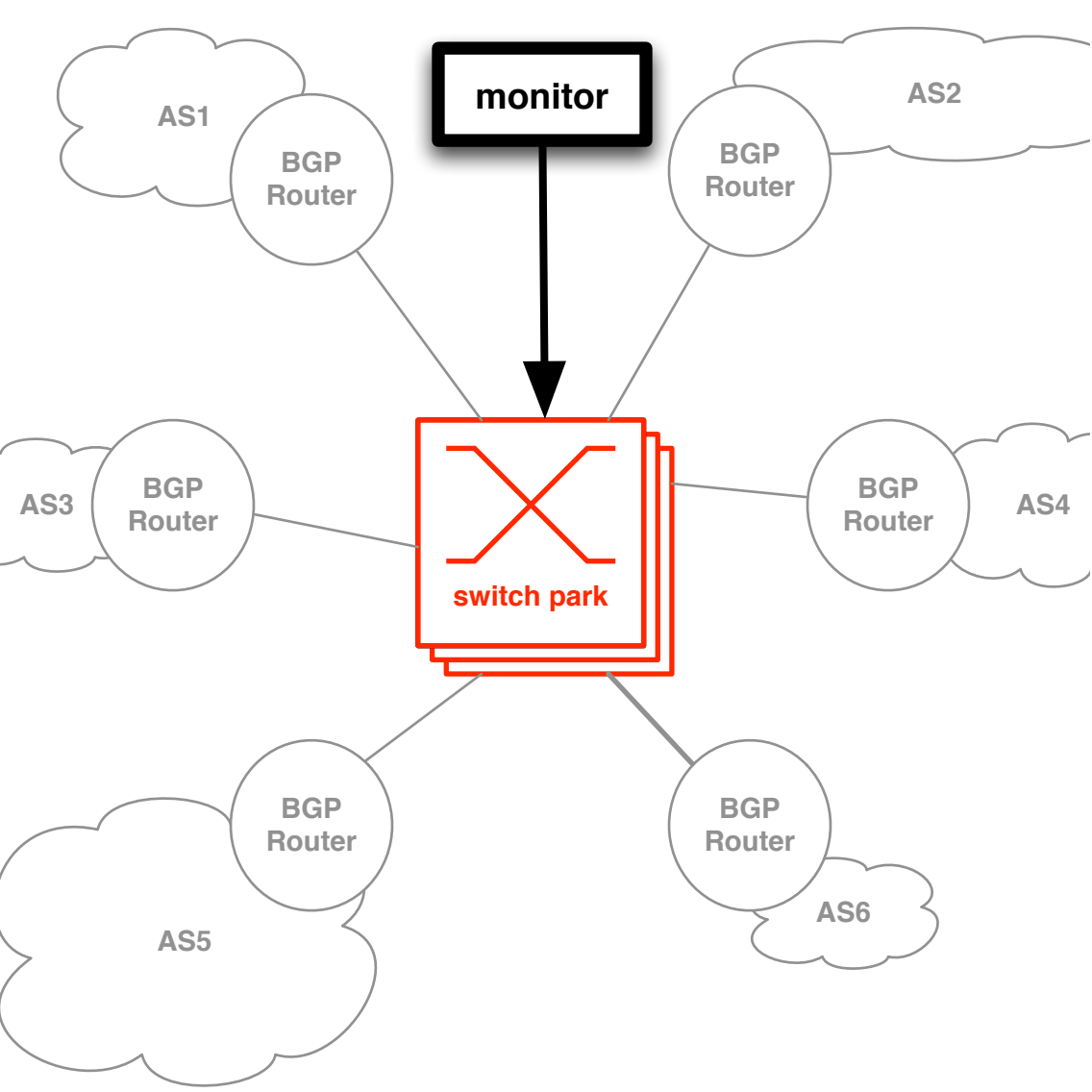


Buttle

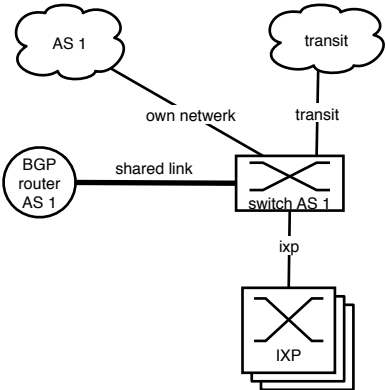


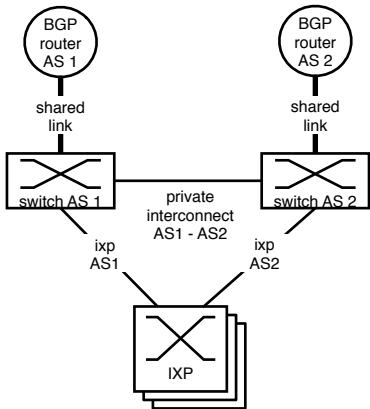


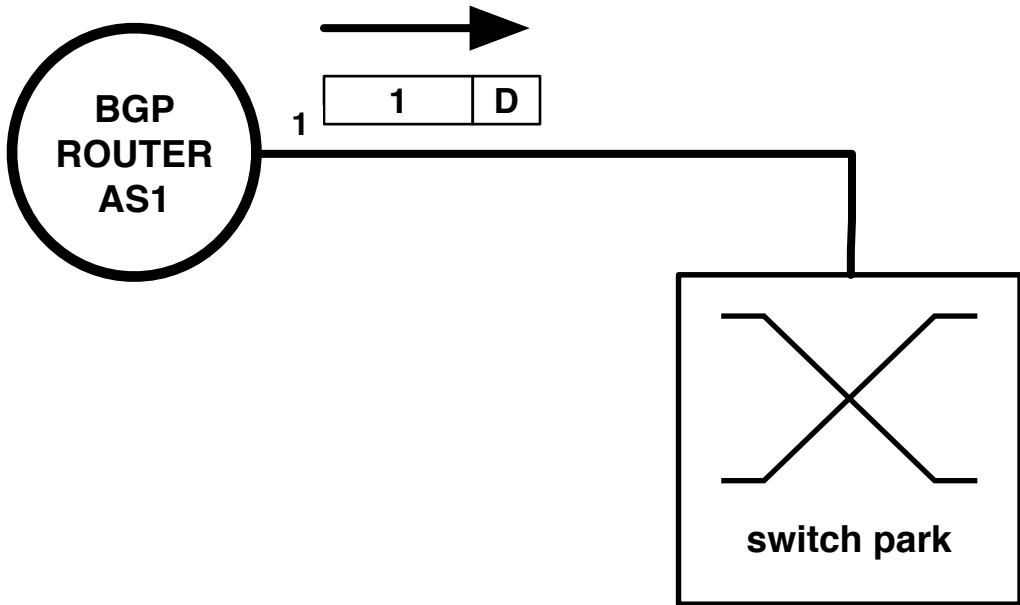


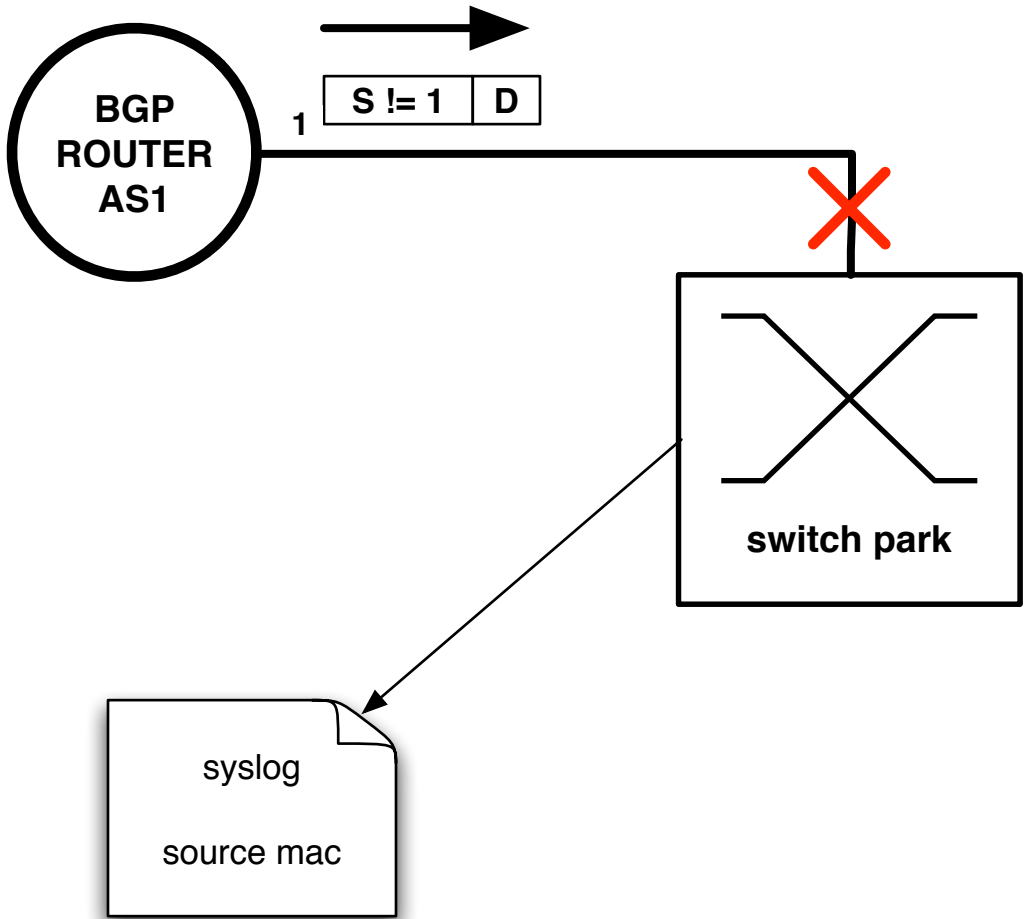


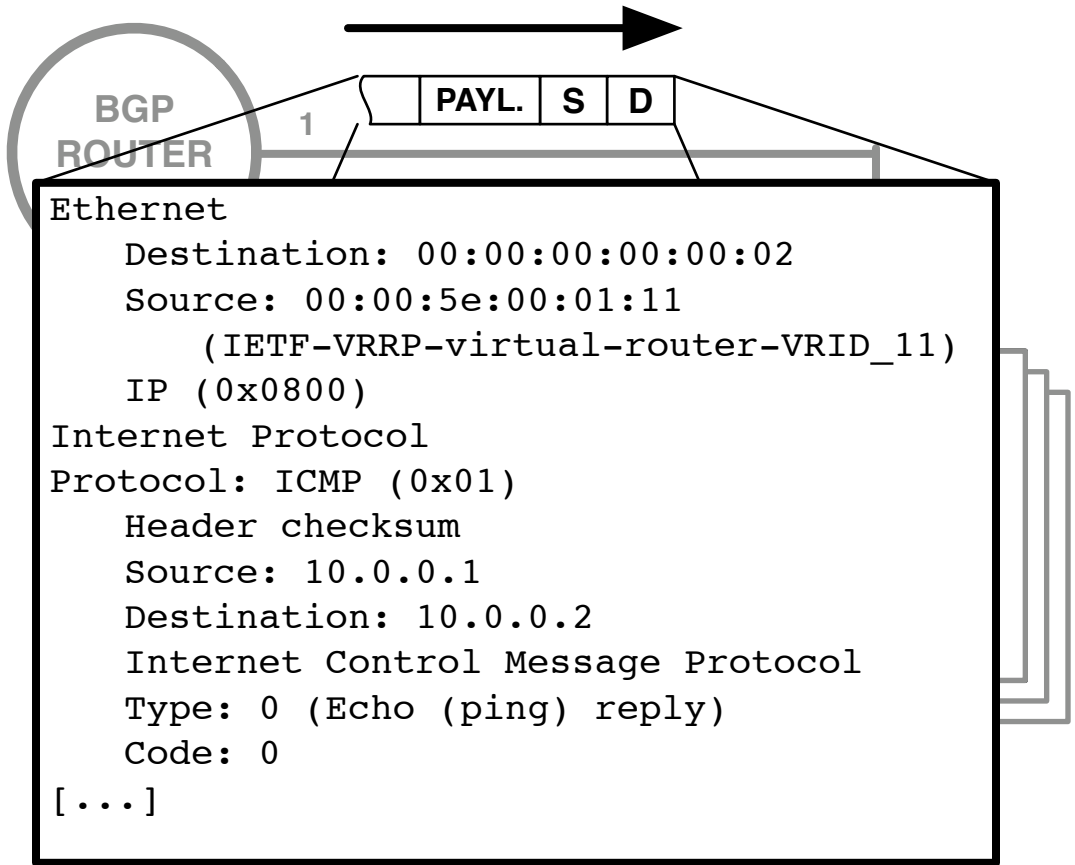
Example #2



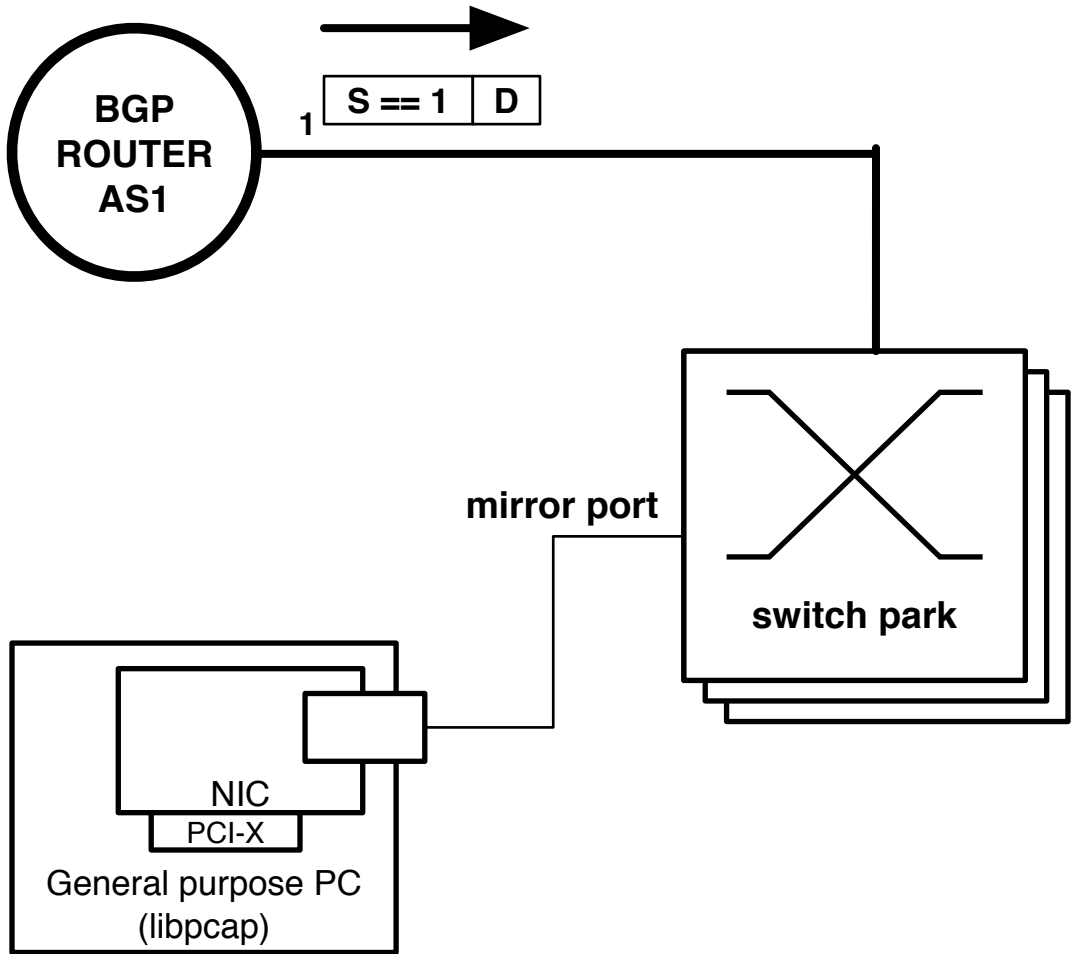


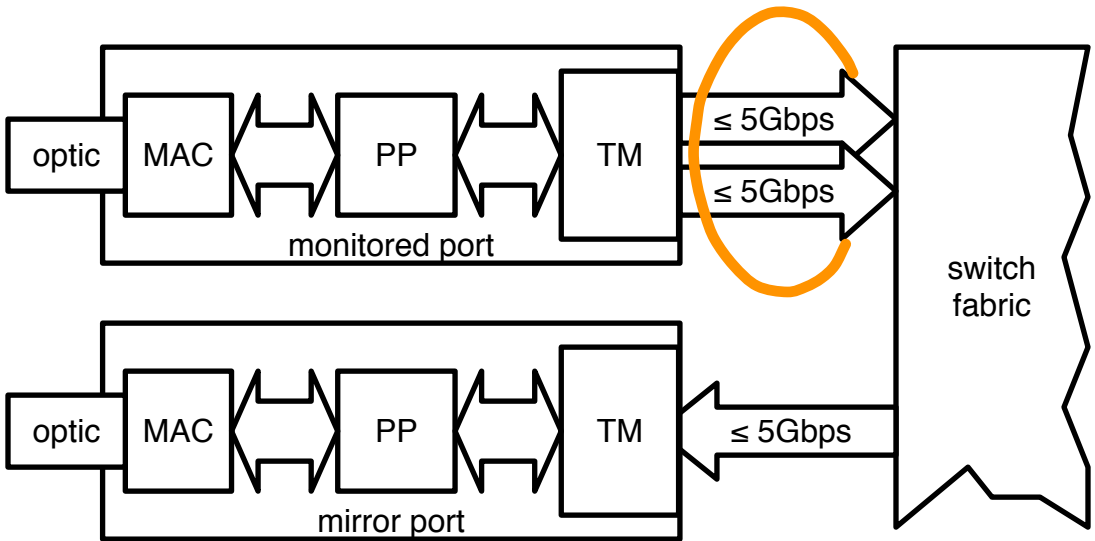






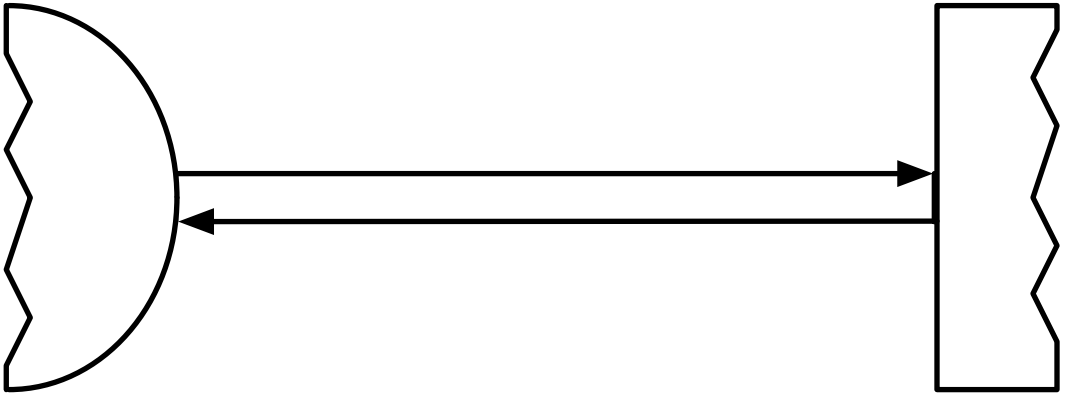
Monitoring





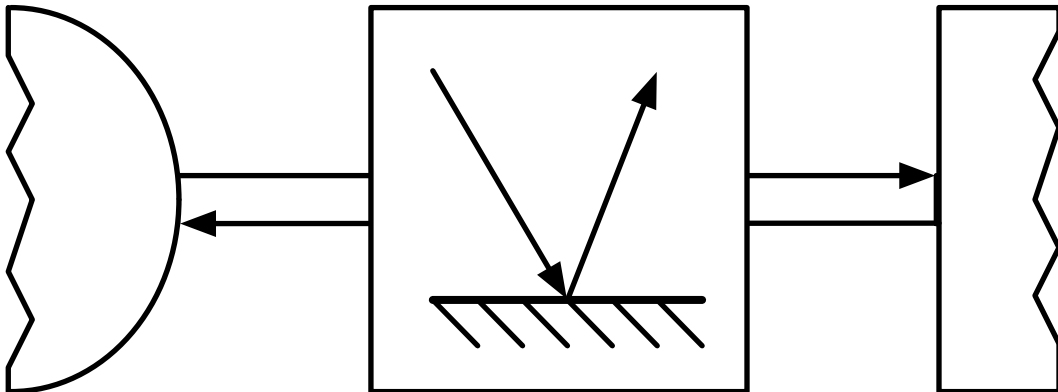
Router

**Ethernet
switch**



Router

**Ethernet
switch**

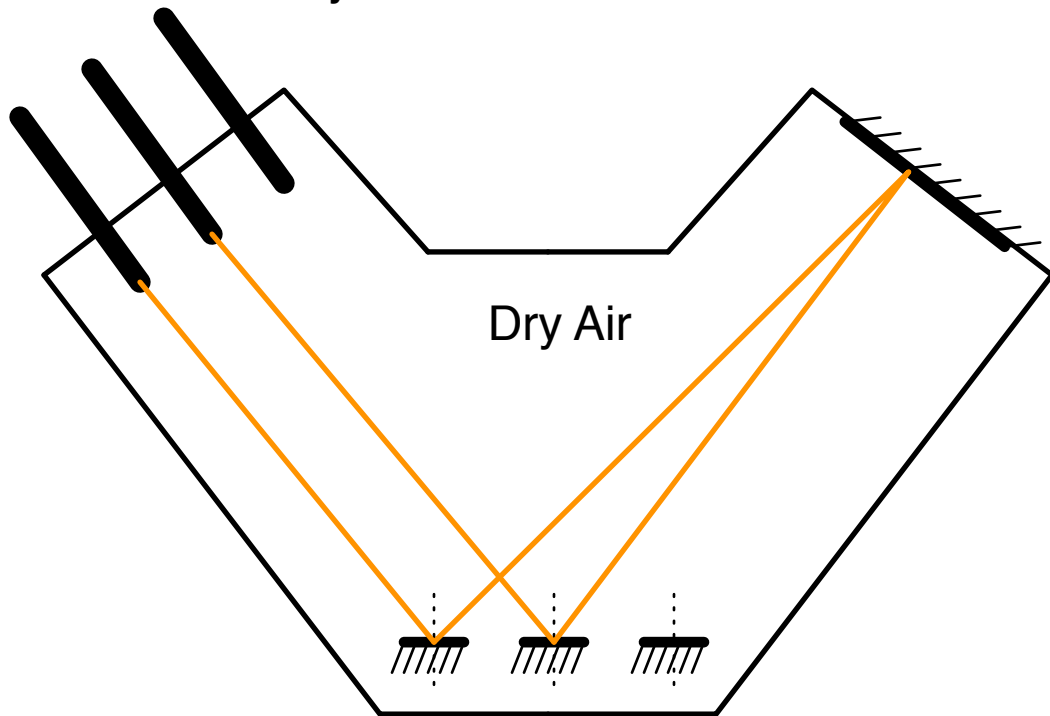


MEMS based Fiber Switch

AKA Photonic Cross Connect (PXC)

Fiber Lens Array

Fixed Mirror

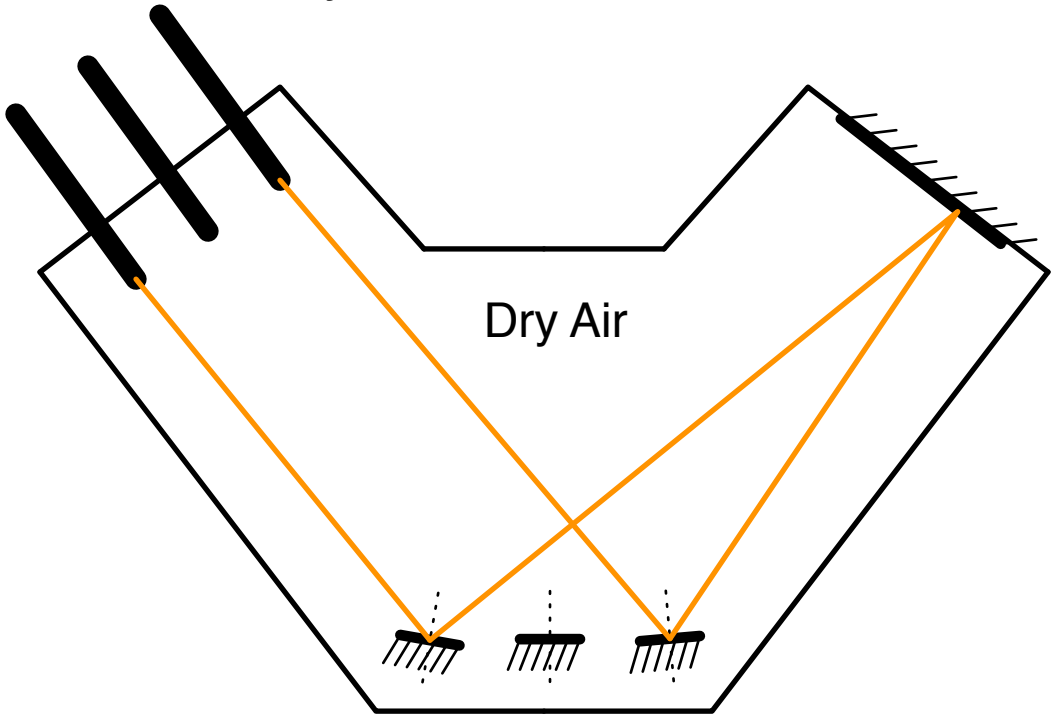


Dry Air

Movable Mirror Array

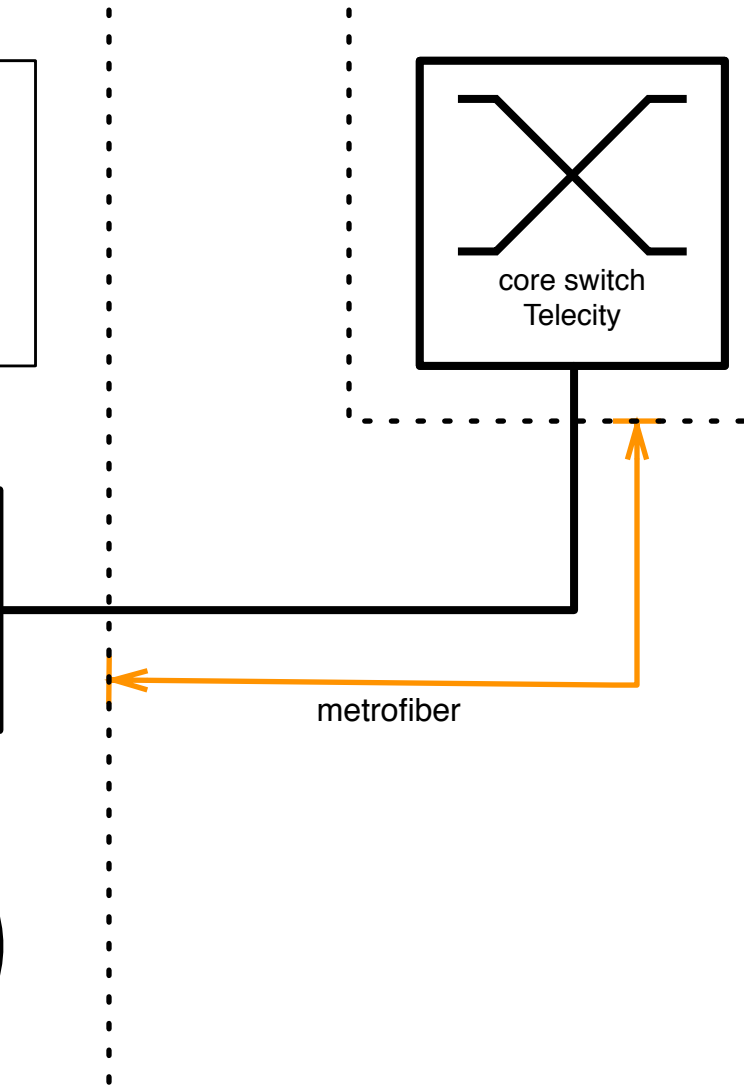
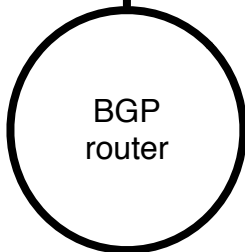
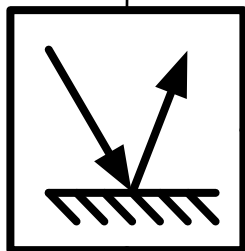
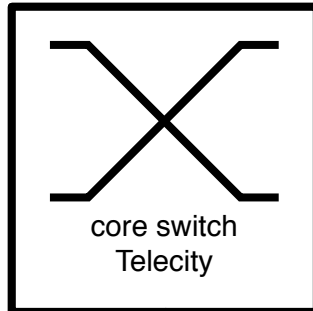
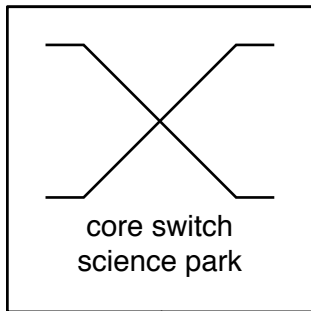
Fiber Lens Array

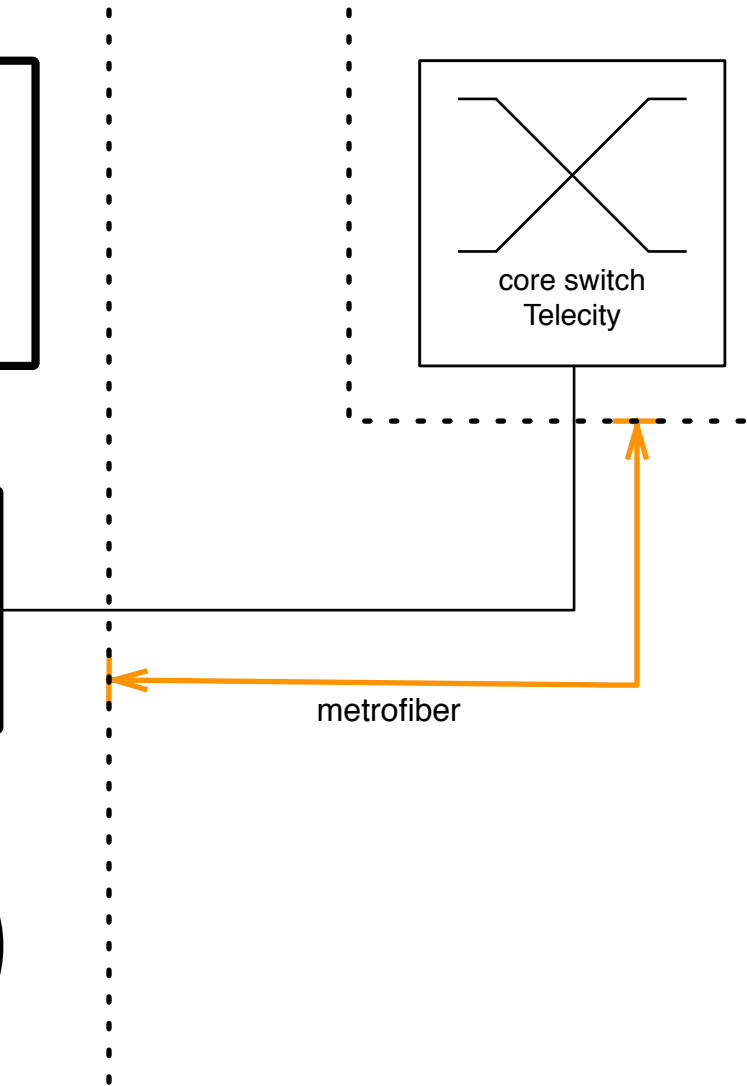
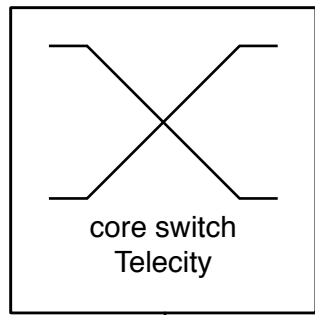
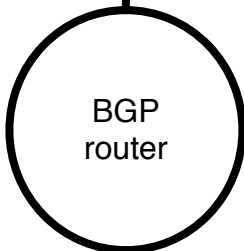
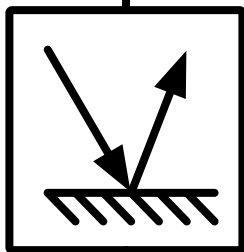
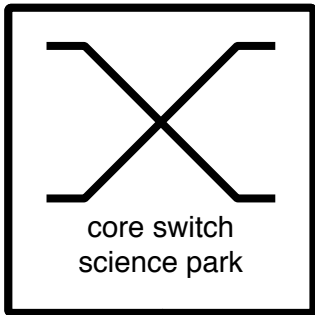
Fixed Mirror

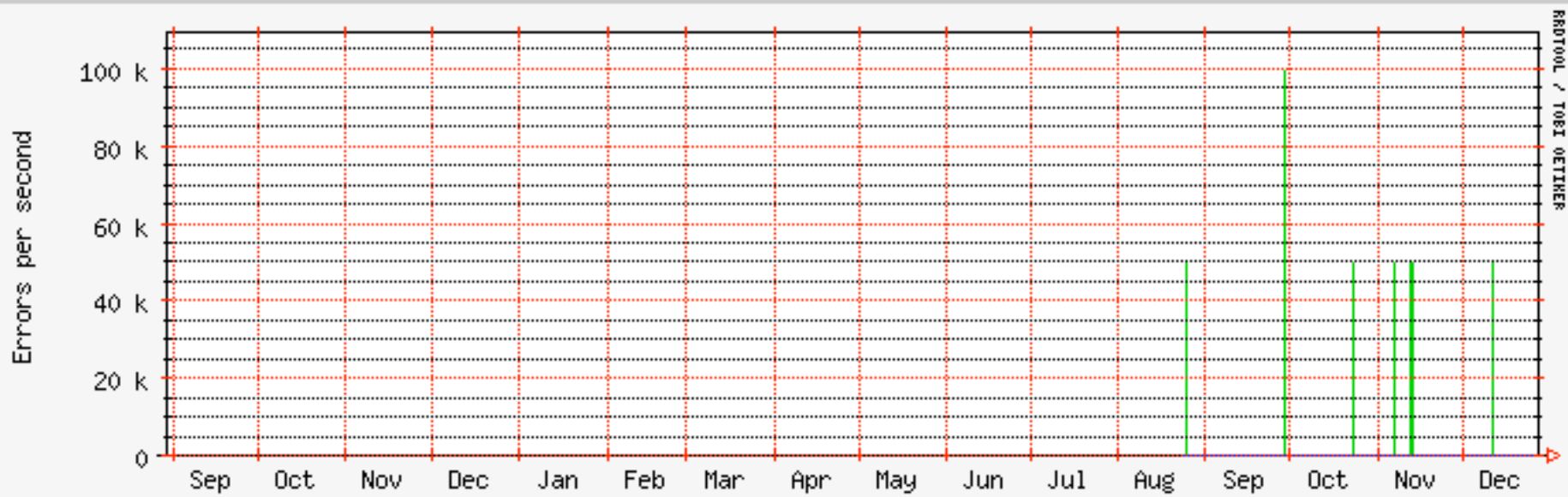


Dry Air

Movable Mirror Array







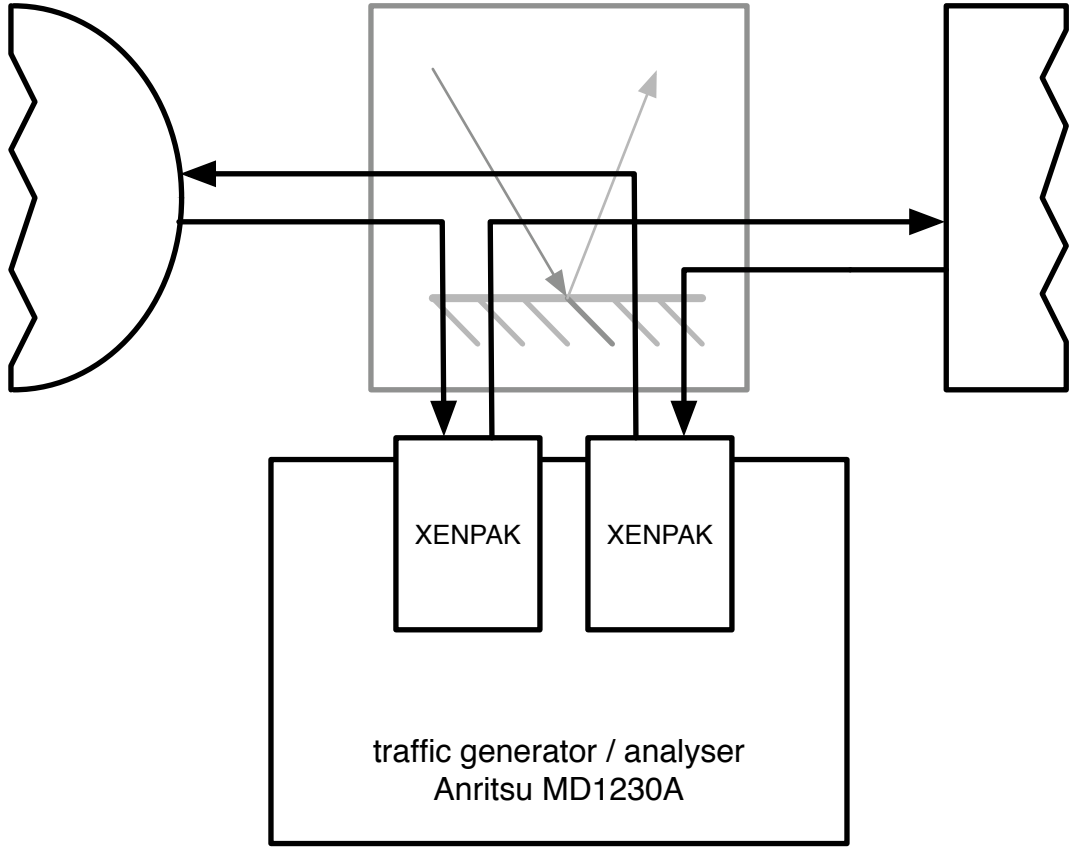
■ Input ■ Output

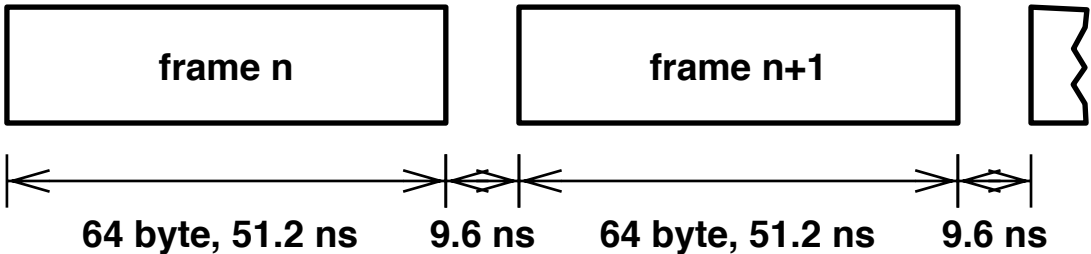
Max In : 99.420 kpkt/s Max Out : 0.000 pkt/s
 Average In : 2.741 kpkt/s Average Out : 0.000 pkt/s
 Current In : 0.000 pkt/s Current Out : 0.000 pkt/s

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Router

**AMS-IX
switch**

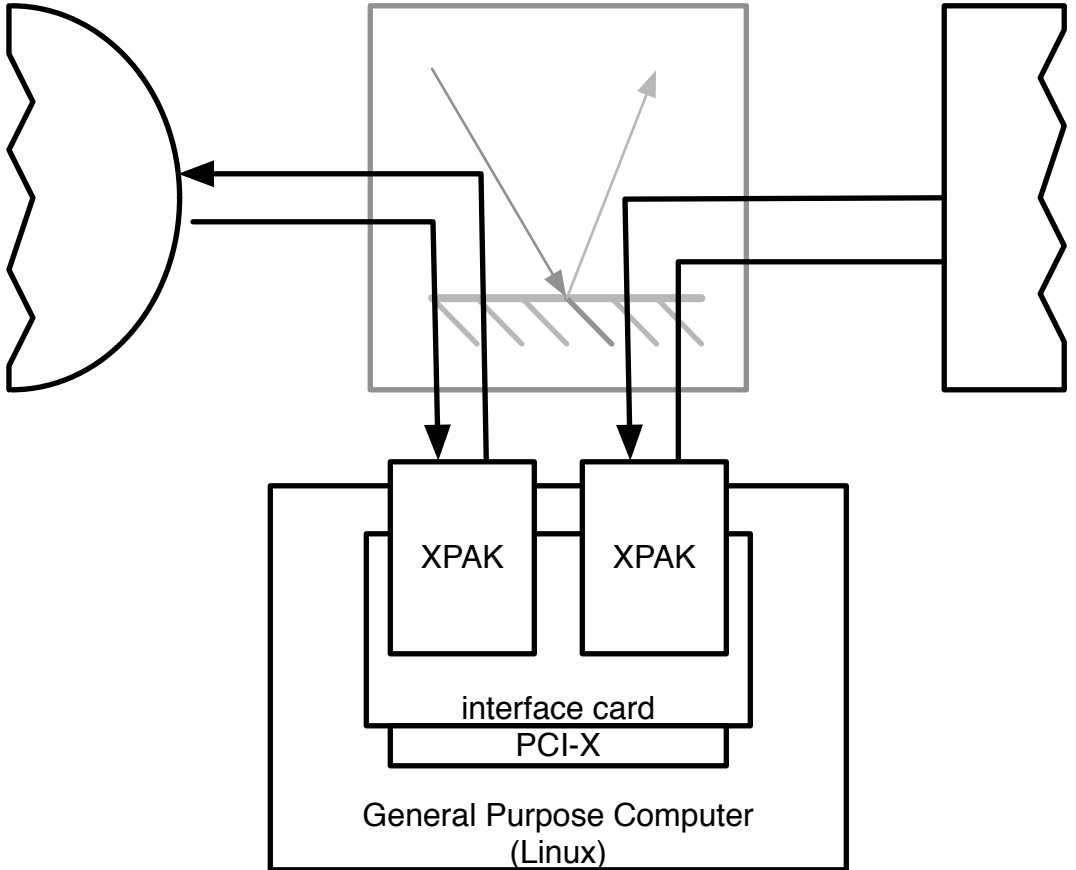


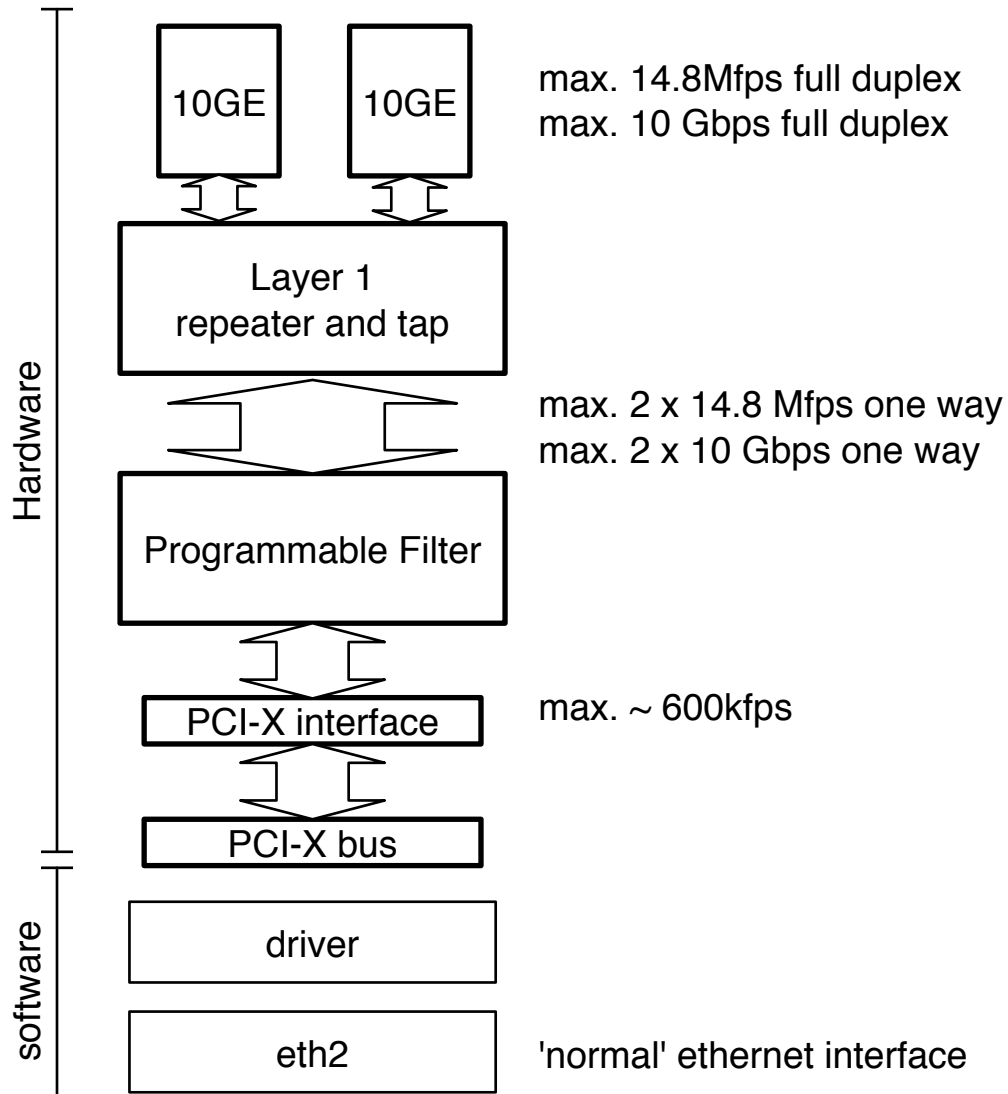


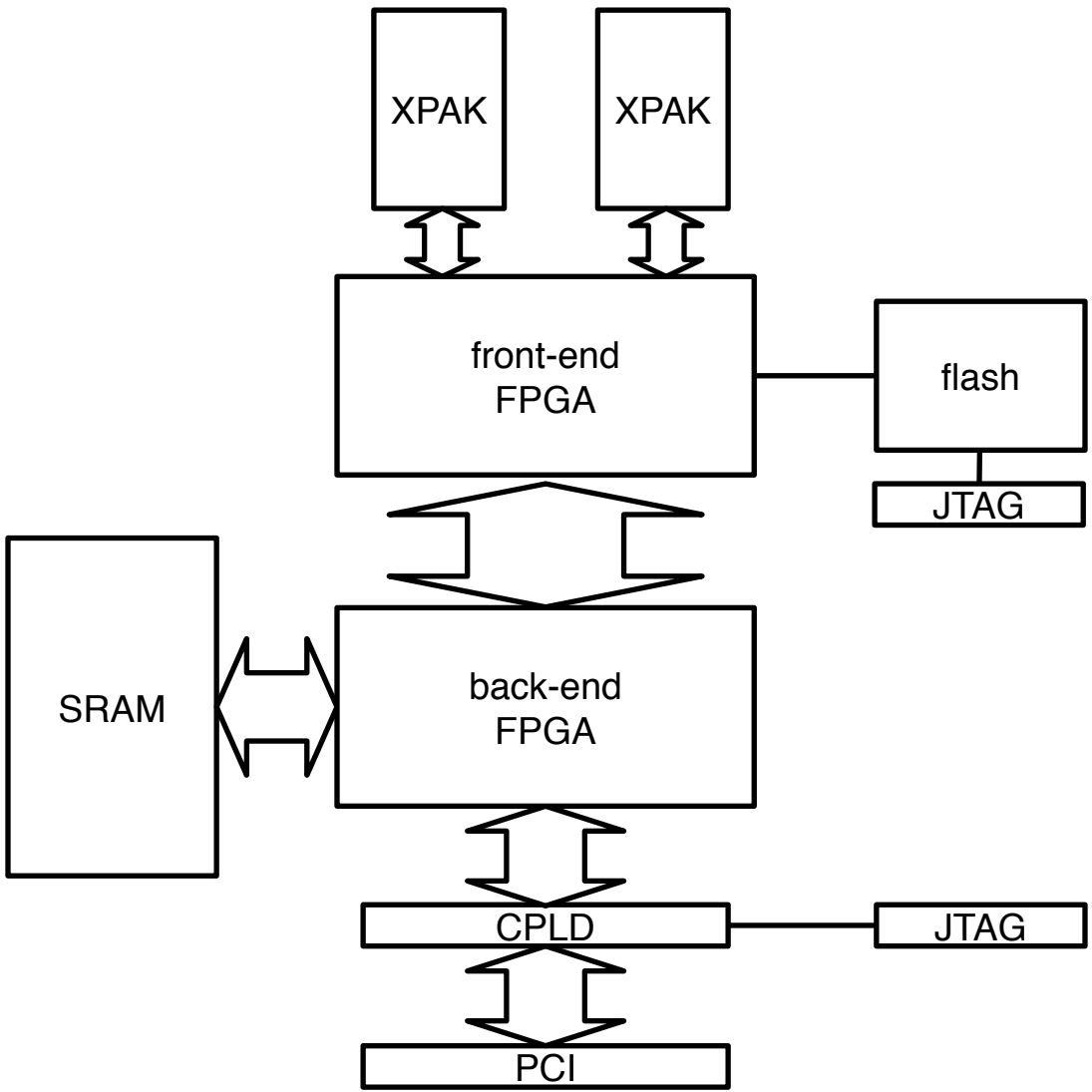
Solution

Router

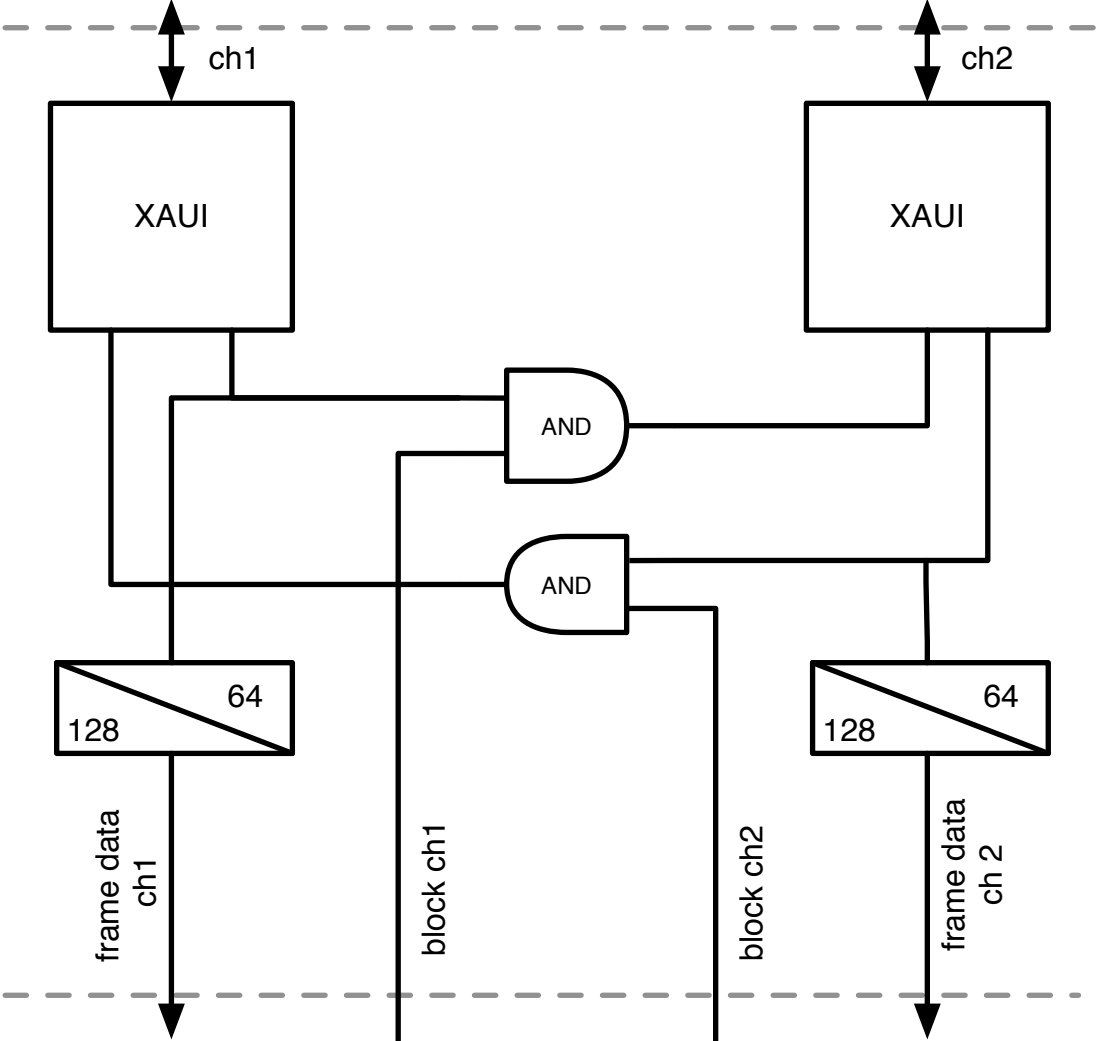
**AMS-IX
switch**







XPAK Transceivers



ch1

ch2

XAUI

XAUI

AND

AND

64

128

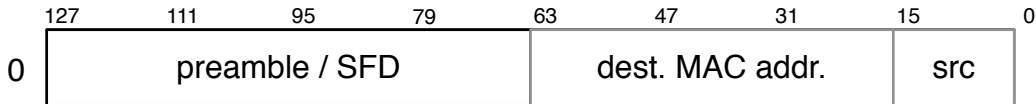
frame data
ch1

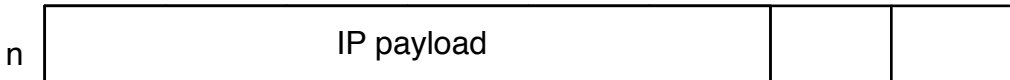
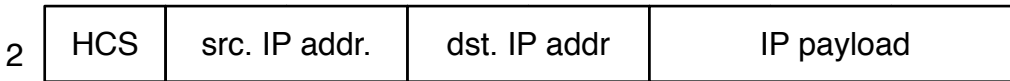
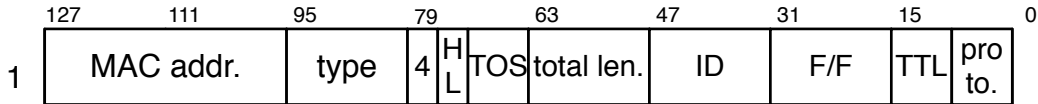
block ch1

block ch2

frame data
ch 2

back-end FPGA





front-end FPGA

frame data

offset

valid

clk

frame data register

R_0

R_1

R_n

C_0

C_1

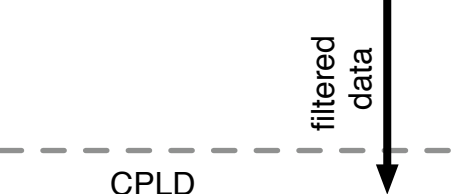
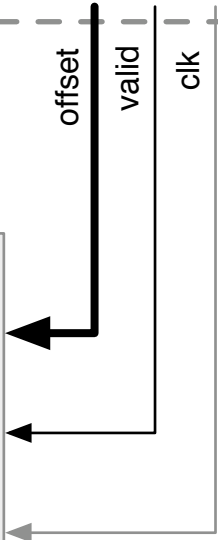
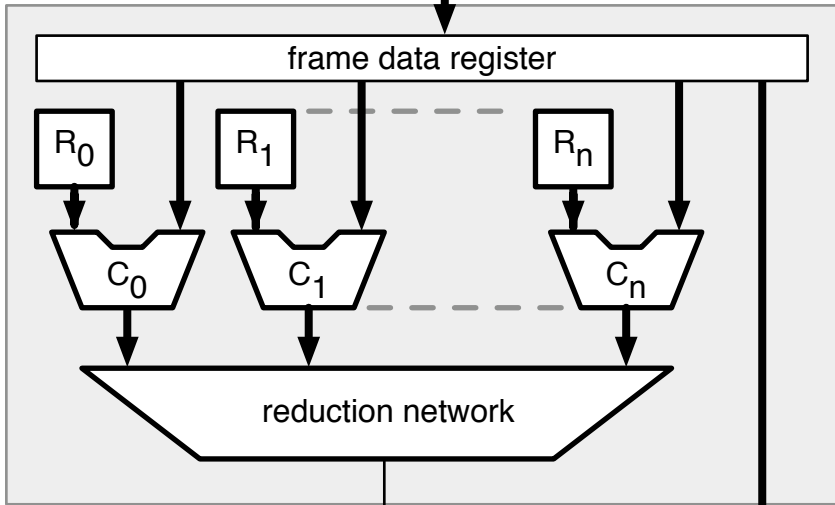
C_n

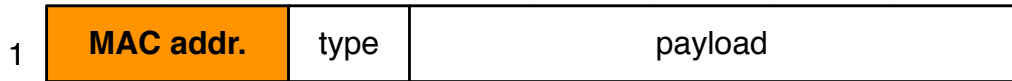
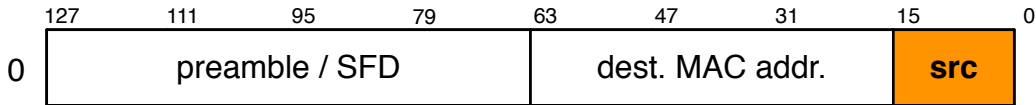
reduction network

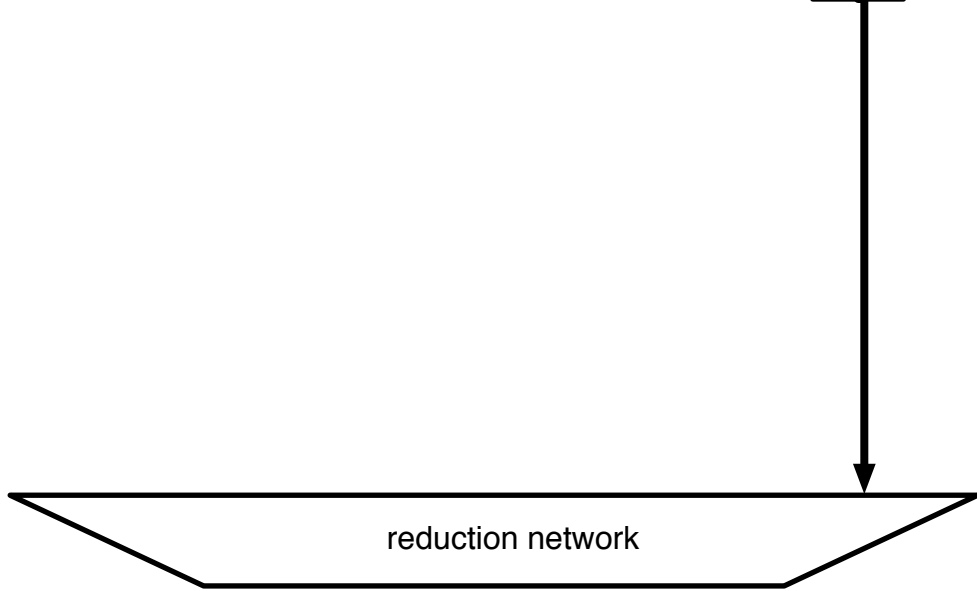
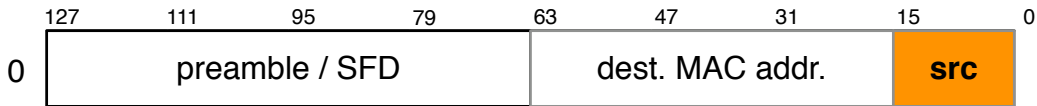
match
memory

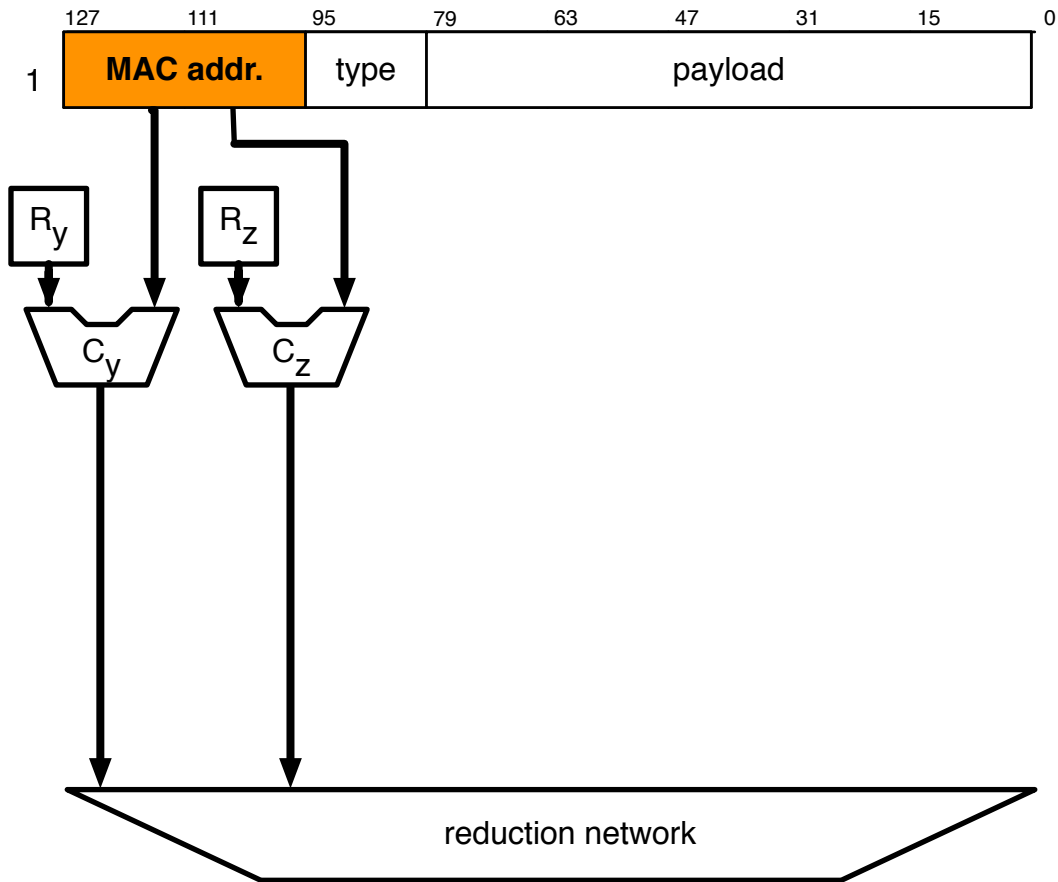
filtered
data

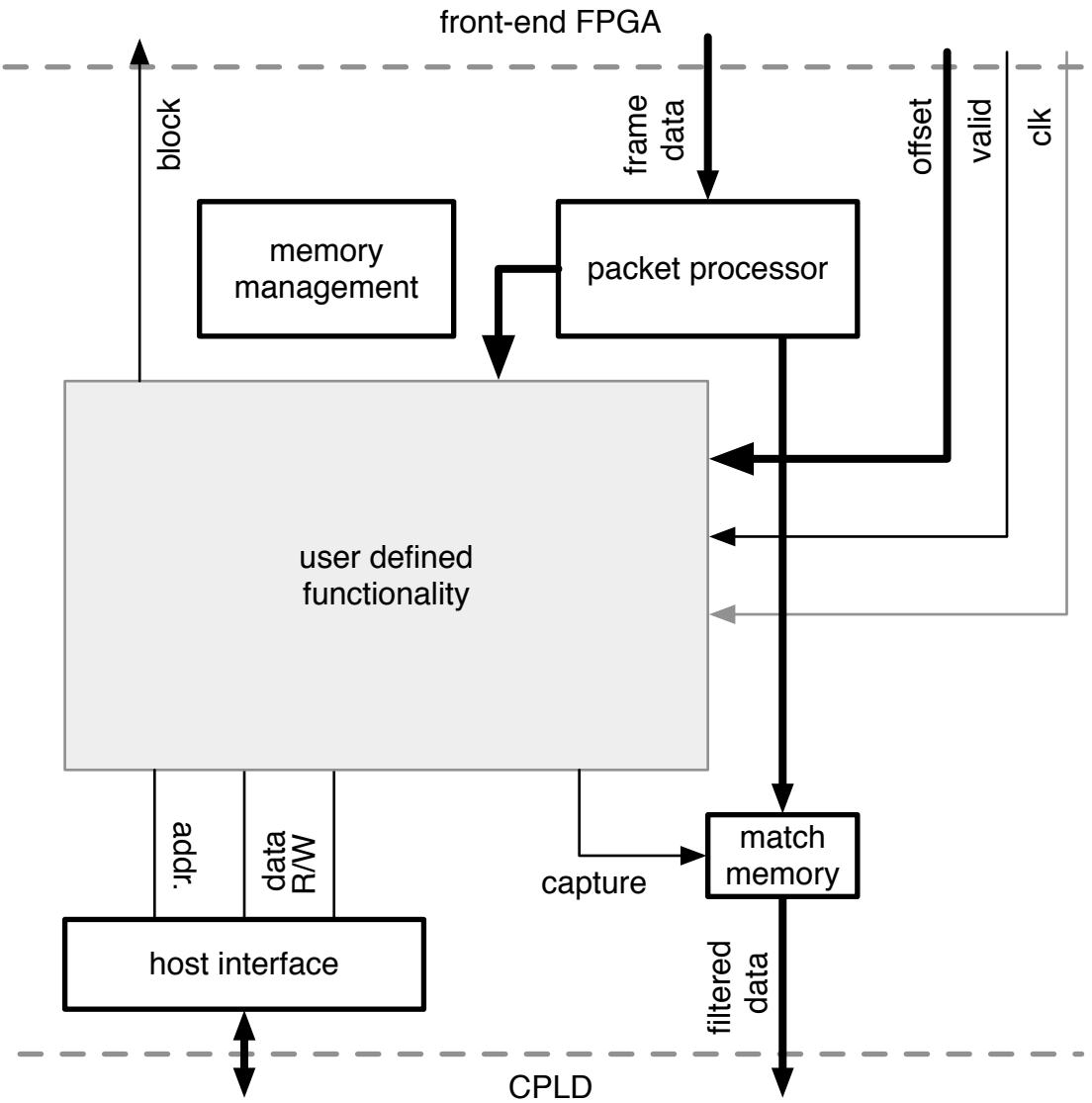
CPLD











front-end FPGA

frame data

offset

valid

clk

frame data register

R_0

R_1

R_n

C_0

C_1

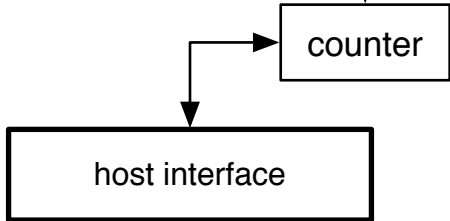
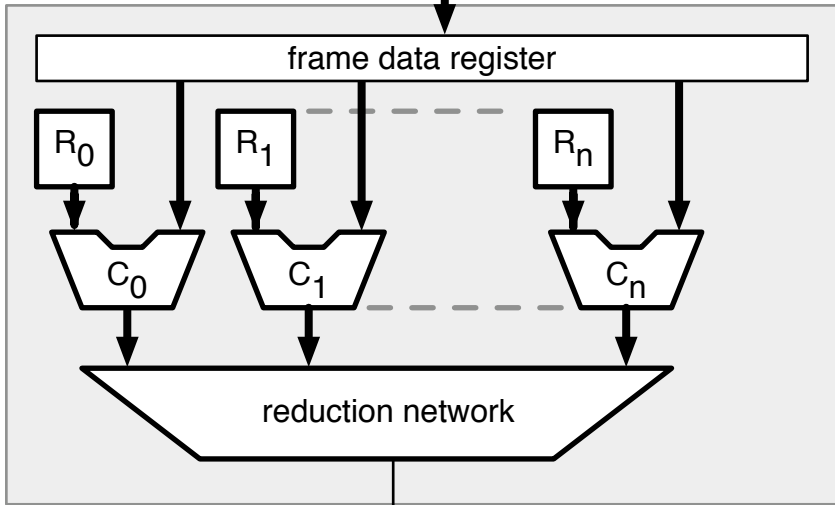
C_n

reduction network

counter

host interface

CPLD



front-end FPGA

frame data

offset

valid

clk

frame data register

R_0

R_1

R_n

C_0

C_1

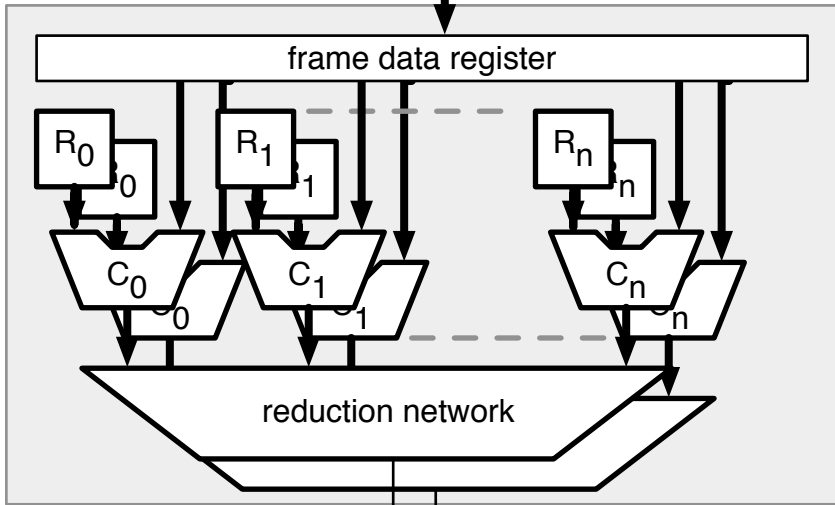
C_n

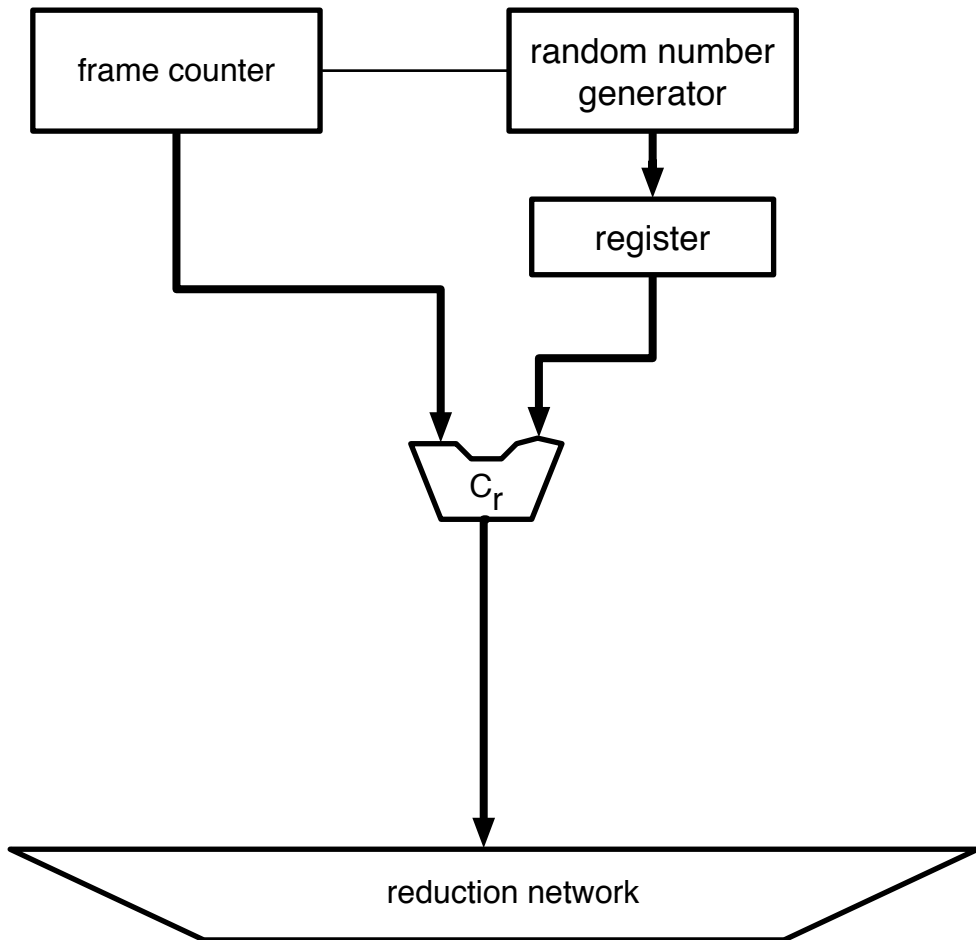
reduction network

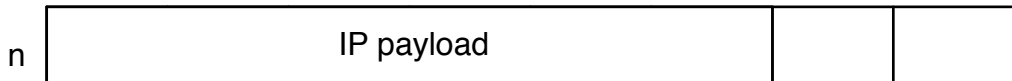
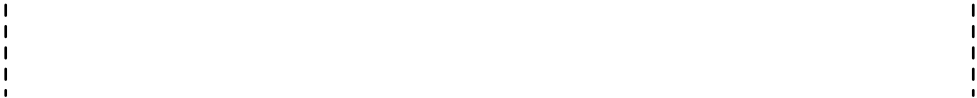
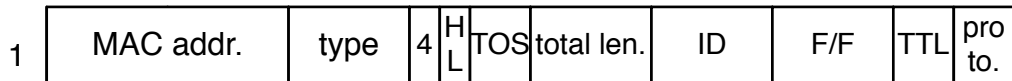
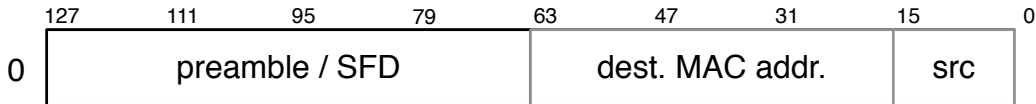
counter

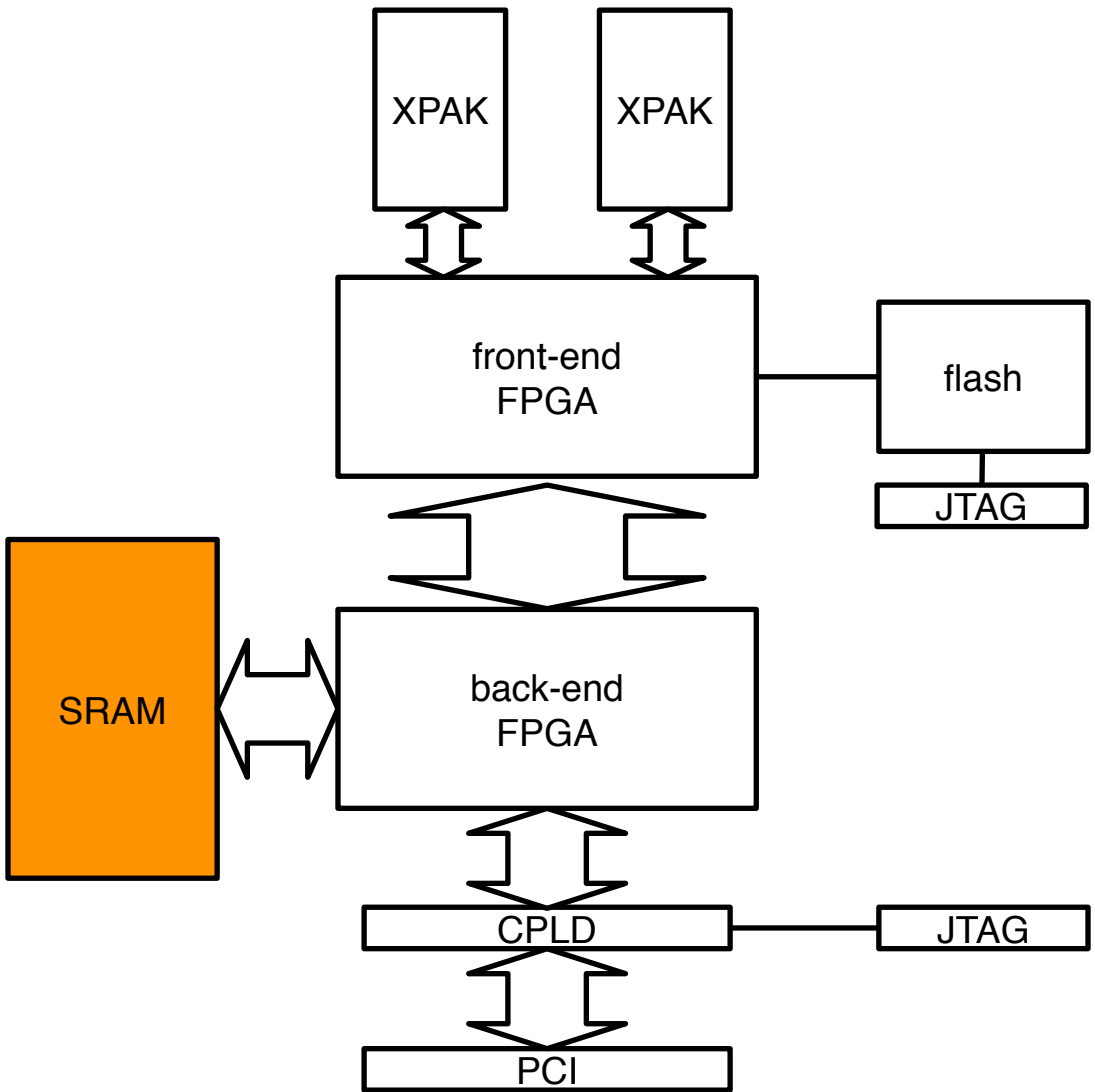
host interface

CPLD









Thank you for your attention