

# Reviving smart card analysis

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SECURITY  
RESEARCH  
LABS

# Executive summary – Modern smart cards should be analyzed

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1. Smart card chips provide the trust base for various applications from banking to ID cards to hardware encryption
  2. The secured chips not only protect secret keys but also shield software and protocols from independent analysis. Vulnerability analysis by manufacturers and contracted labs has overlooked bugs numerous times, so independent analysis is needed for software protected by smart cards
  3. This talk describes a method for extracting smart card software for analysis through semi-automated reverse-engineering of circuits and optical memory read-out
  4. The potential for code read-out affects most modern smart cards. Mitigating it requires stronger memory encryption combined with smarter key storage
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# Agenda

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- ▶ **Smart card basics**
  - Reverse-engineering memory encryption
  - Mitigation measures
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# A few smart cards chips cover numerous security domains

## Smart card applications



Payment cards, electronic IO cards, access badges



Trusted Platform Modules (TPM)



Device and accessory identification



SIM cards, NFC secure elements

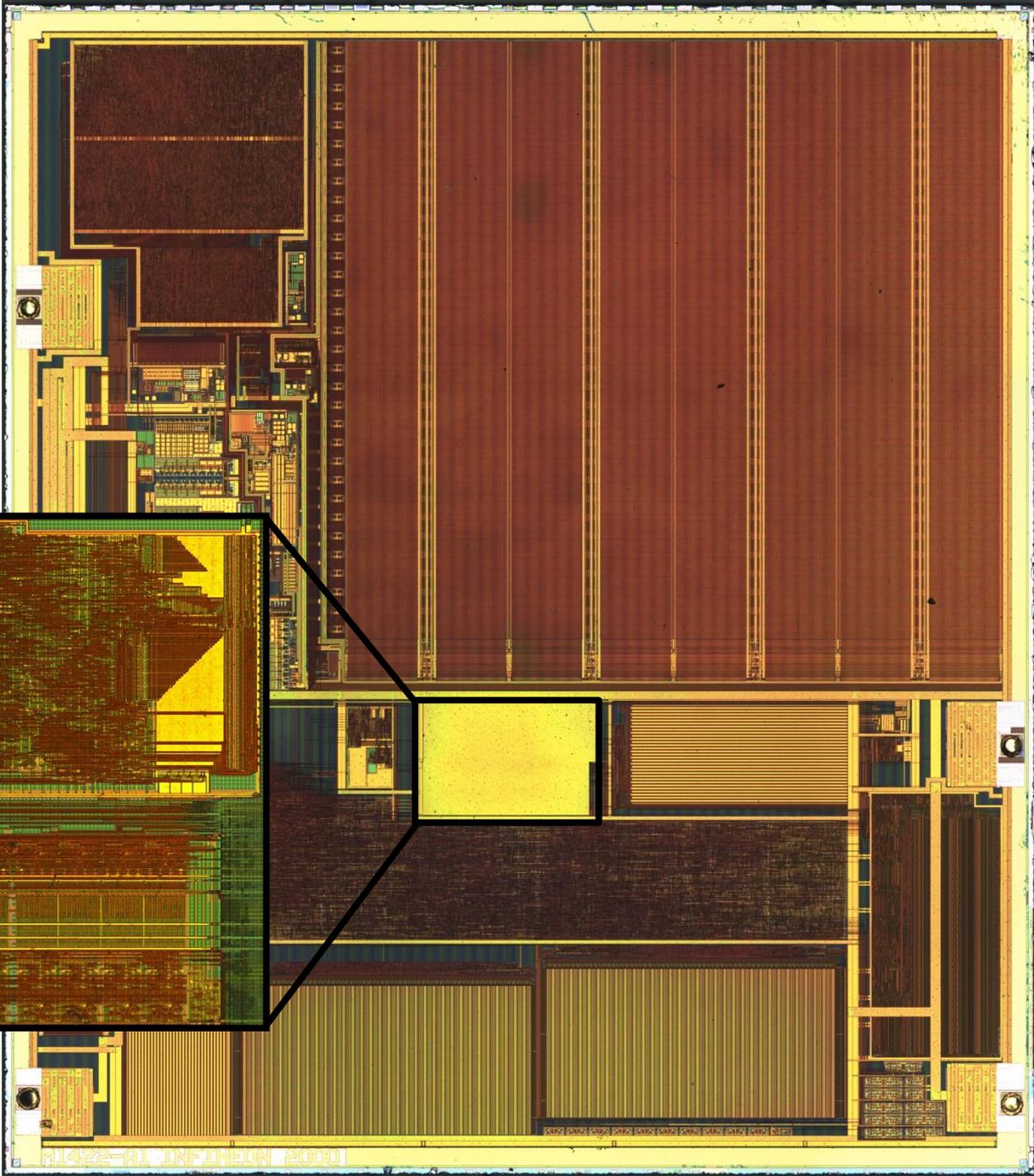
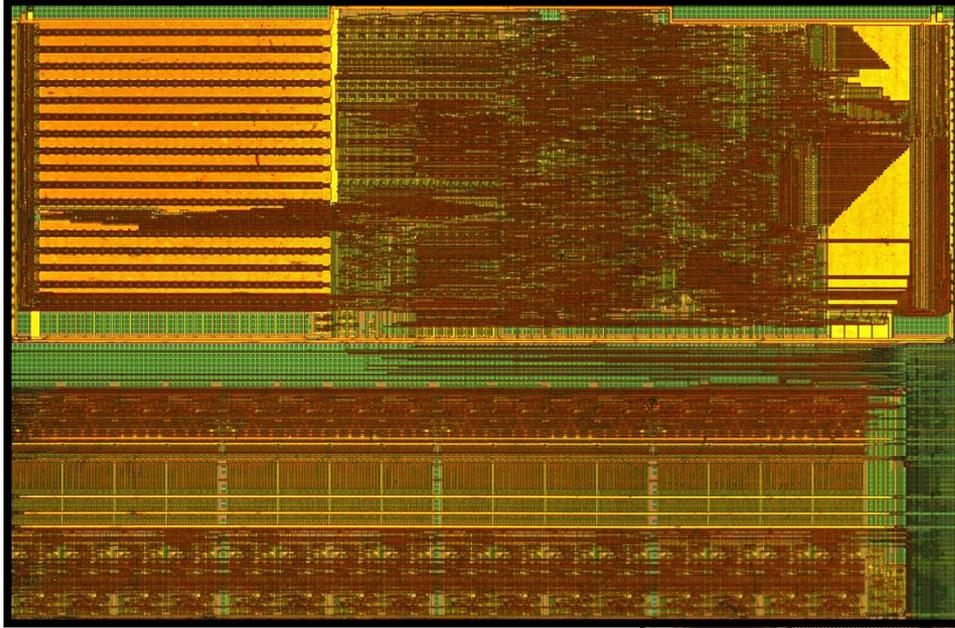


Content protection

### Bulk risk

- Only a handful of manufacturers provide smart cards
- Therefore, every card compromise affects numerous applications

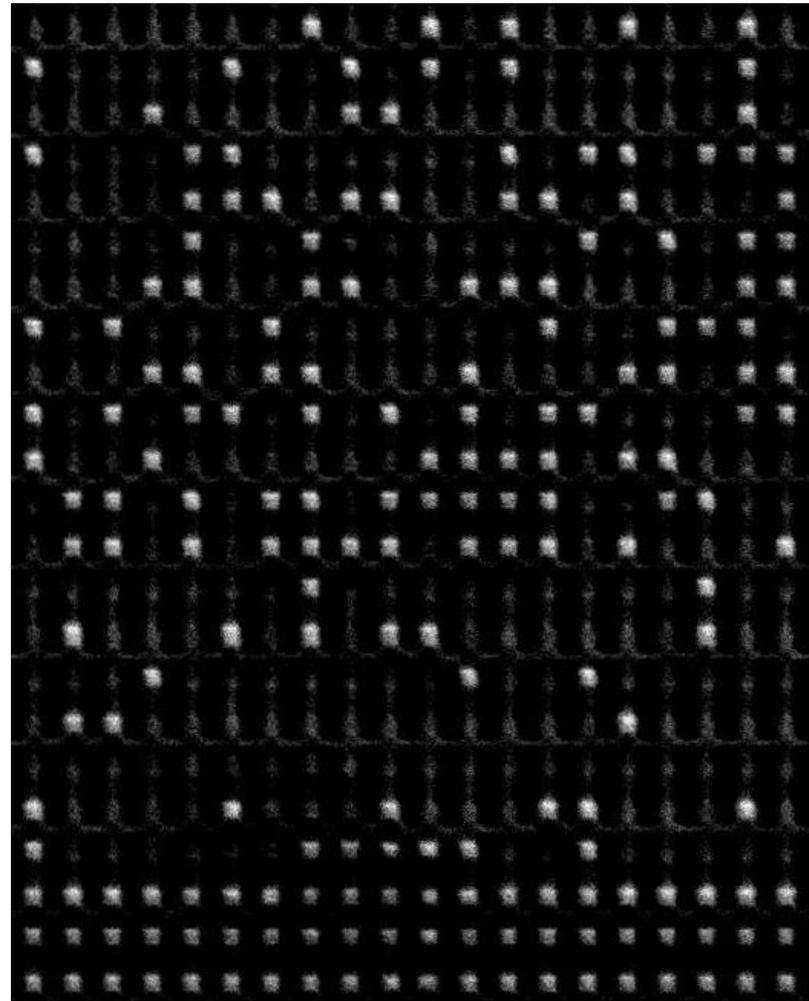
Smart  
card  
chip



# Unencrypted ROM memory can be read optically



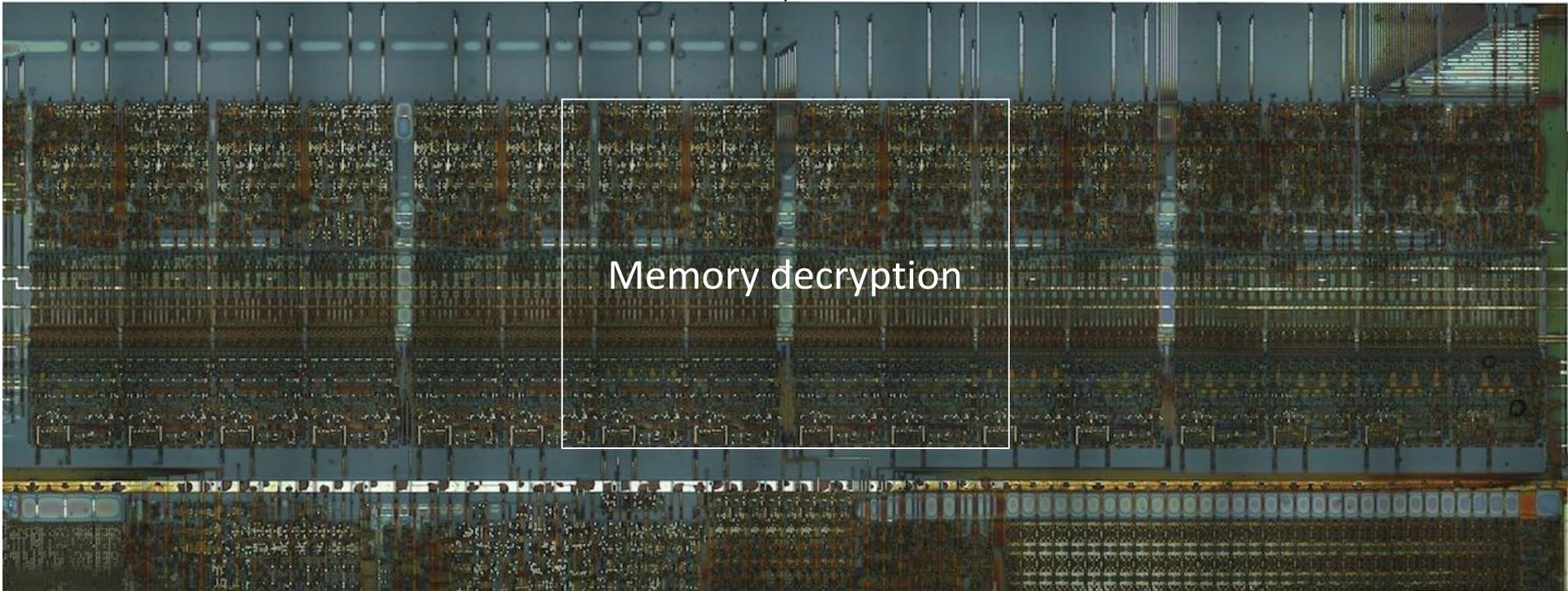
**Metal-masked ROM**



**Ion-implanted ROM (after staining)**

# Smart cards protect code and data with memory encryption

Memories



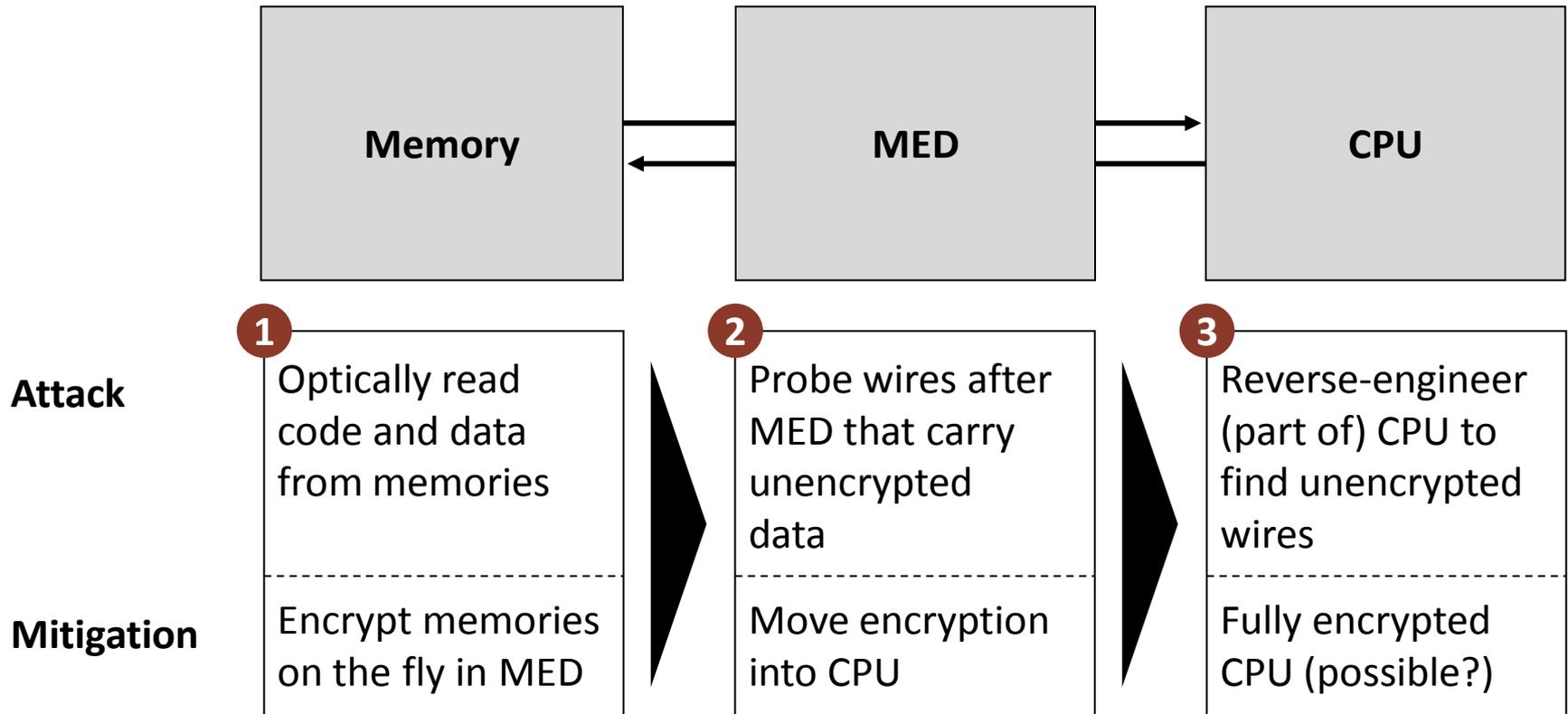
Memory decryption



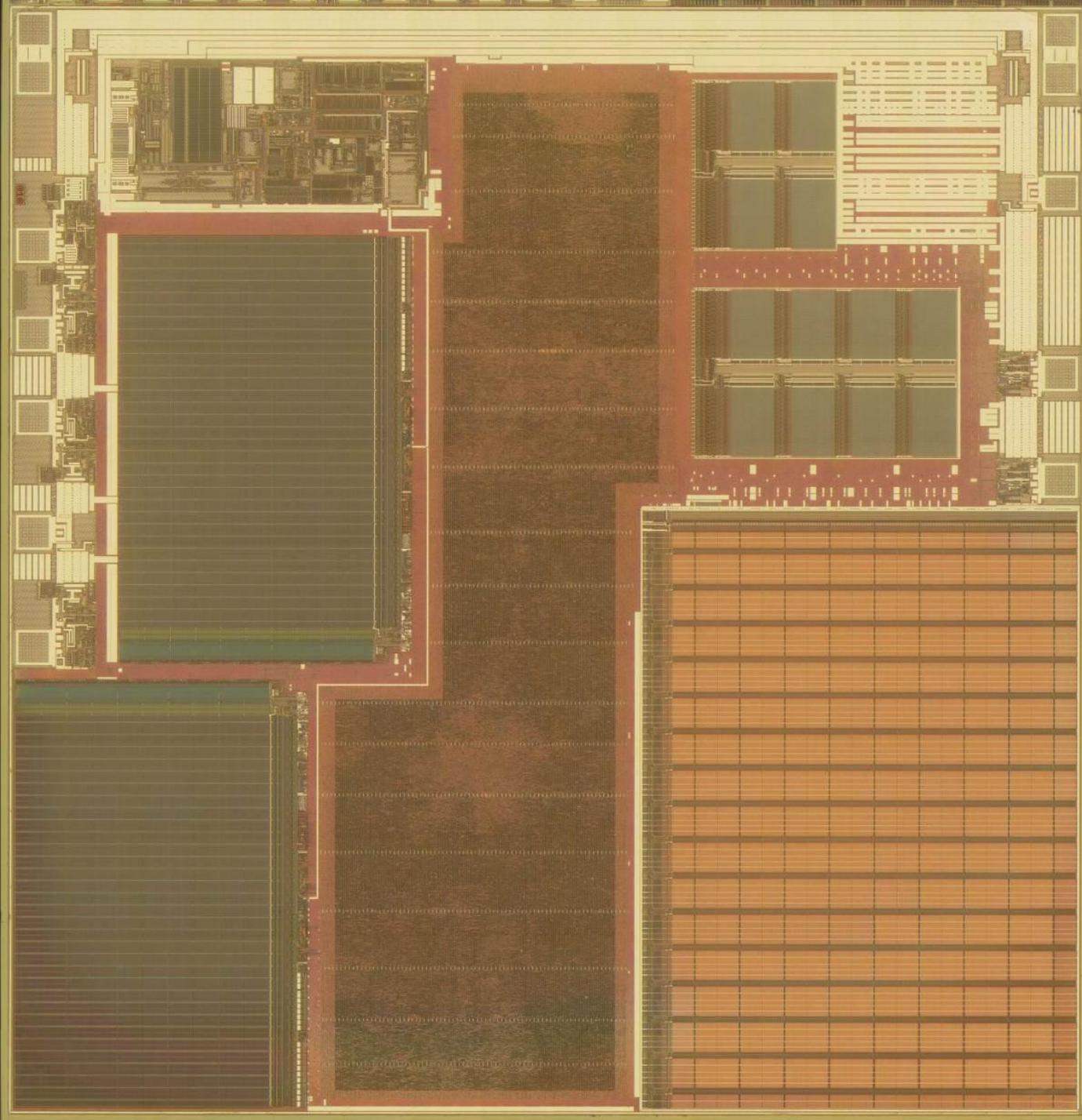
CPU

▶ Newer smart cards hide the decryption in the CPU

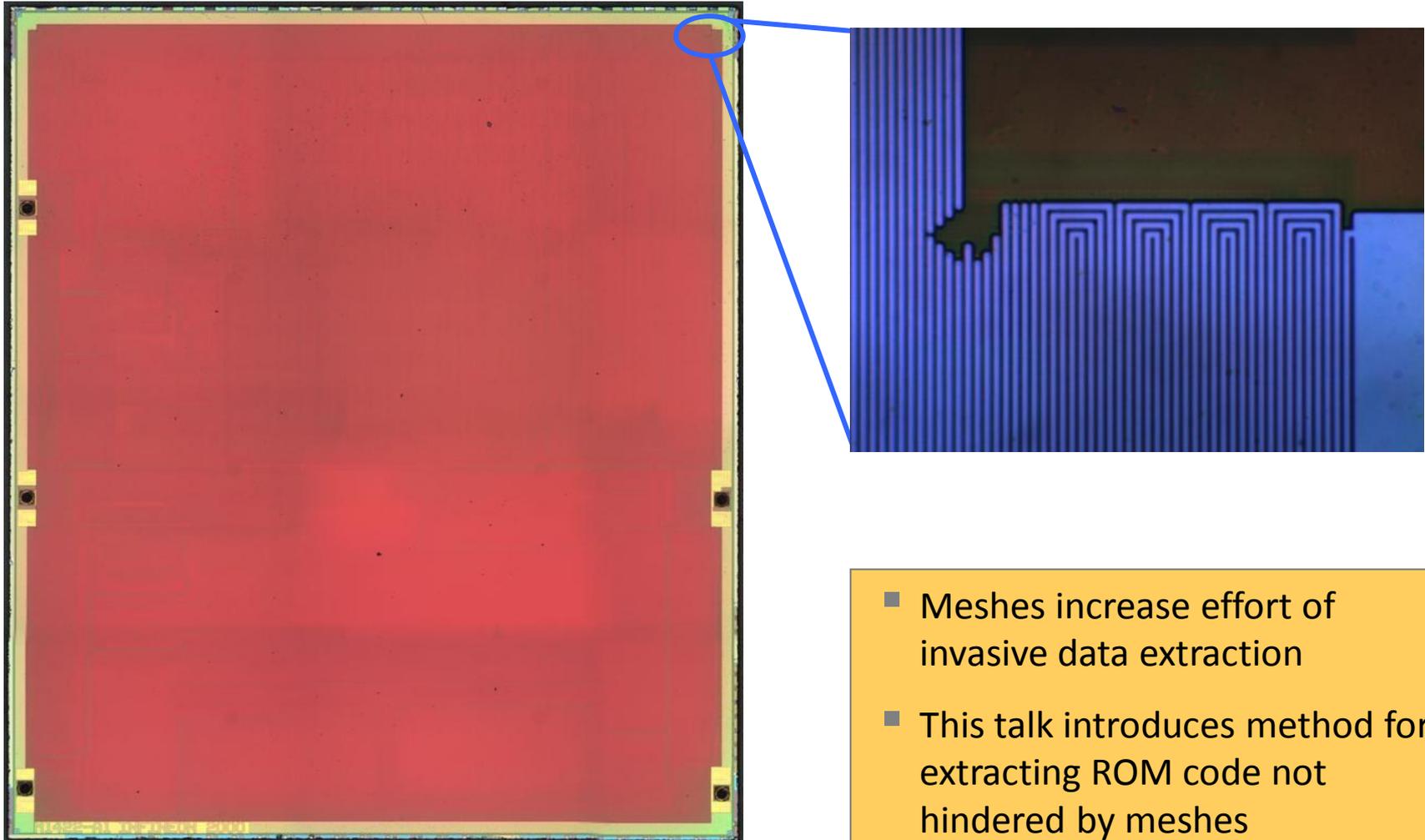
# Recent design iterations moved cryptography deeper into chips



Smart card  
with  
memory  
encryption  
in CPU core



# Protection meshes create additional complexity for invasive attacks



- Meshes increase effort of invasive data extraction
- This talk introduces method for extracting ROM code not hindered by meshes

# Agenda

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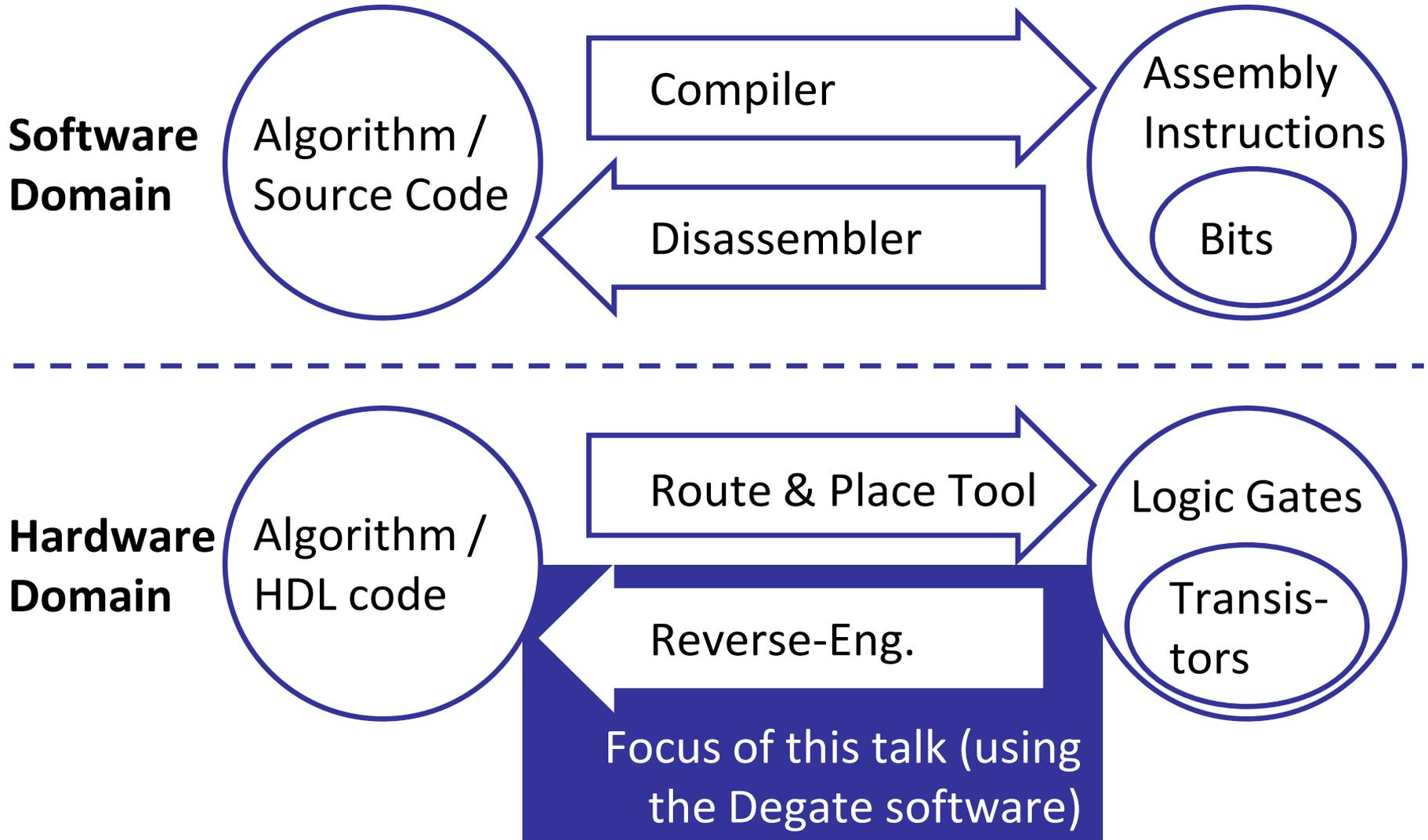
- Smart card basics

- **Reverse-engineering memory encryption**

- Mitigation measures

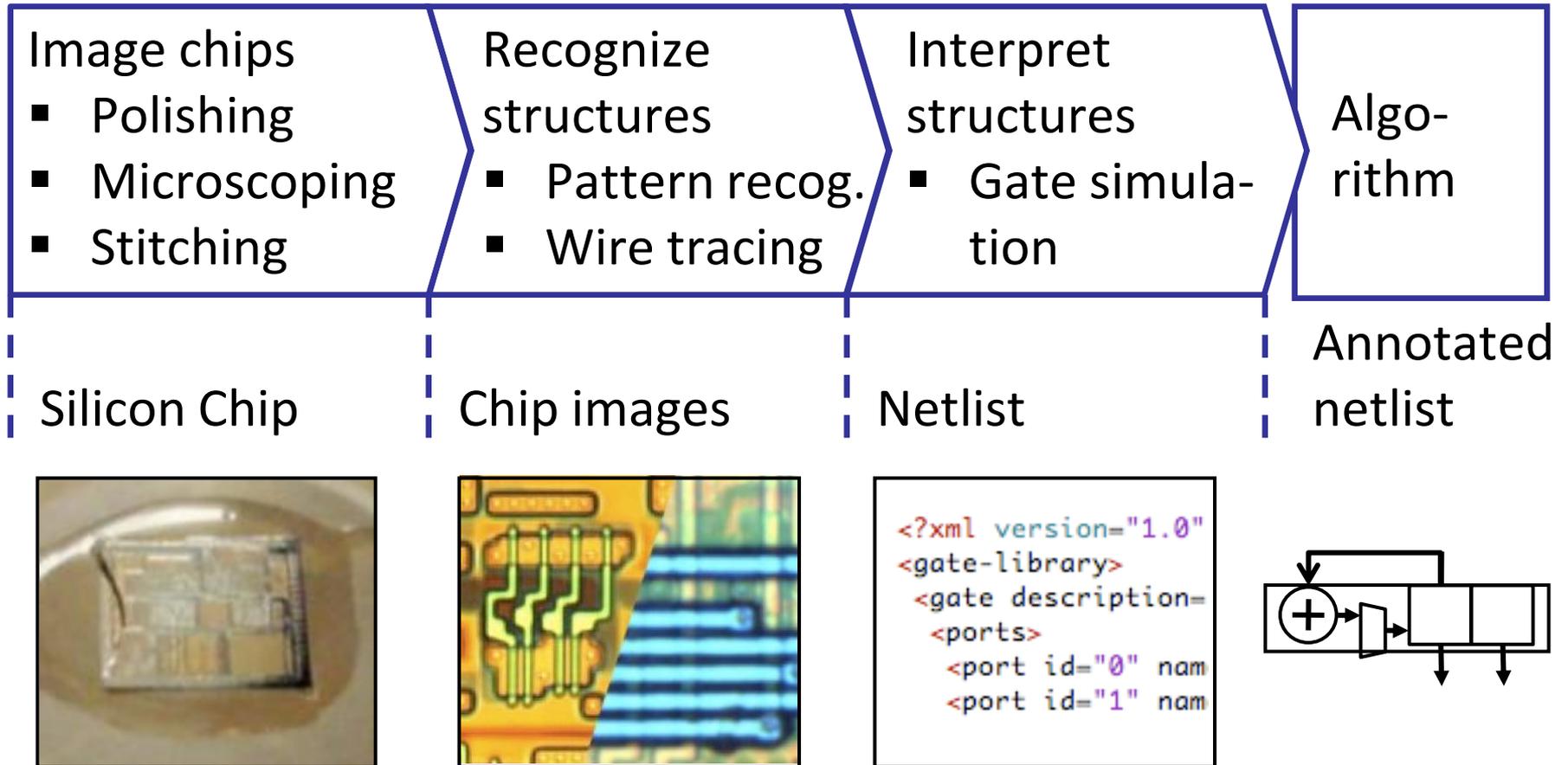
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# Researchers need better tools for finding algorithms in hardware



# Algorithms can be extracted from chips in a 3-step process

## Silicon disassembling process



# Demo: Reverse-engineering with Degate

The screenshot displays the Degate software interface for reverse-engineering logic gates. The main window shows a logic diagram with various gates and their connections. Two windows are open in the foreground:

**Logic gates**

Short Name	#	Width	Height	Fill color	Frame color	Description
01-FF	58	272	134	Black	Red	D-Q-FlipFlop
02-FF	11	343	134	Black	White	D-Q-FlipFlop with rst
03-FF	17	343	133	Black	White	D-Q-FlipFlop with rts
04-BUF	5	226	128	Black	White	
05-3XOR	13	249	133	Black	White	
06-2-XNOR	12	133	133	Black	White	

**Edit gate**

Entity Behaviour Layout

Short name: 02-FF  
Description: D-Q-FlipFlop with rst  
Logic Class: flipFlop (generic)

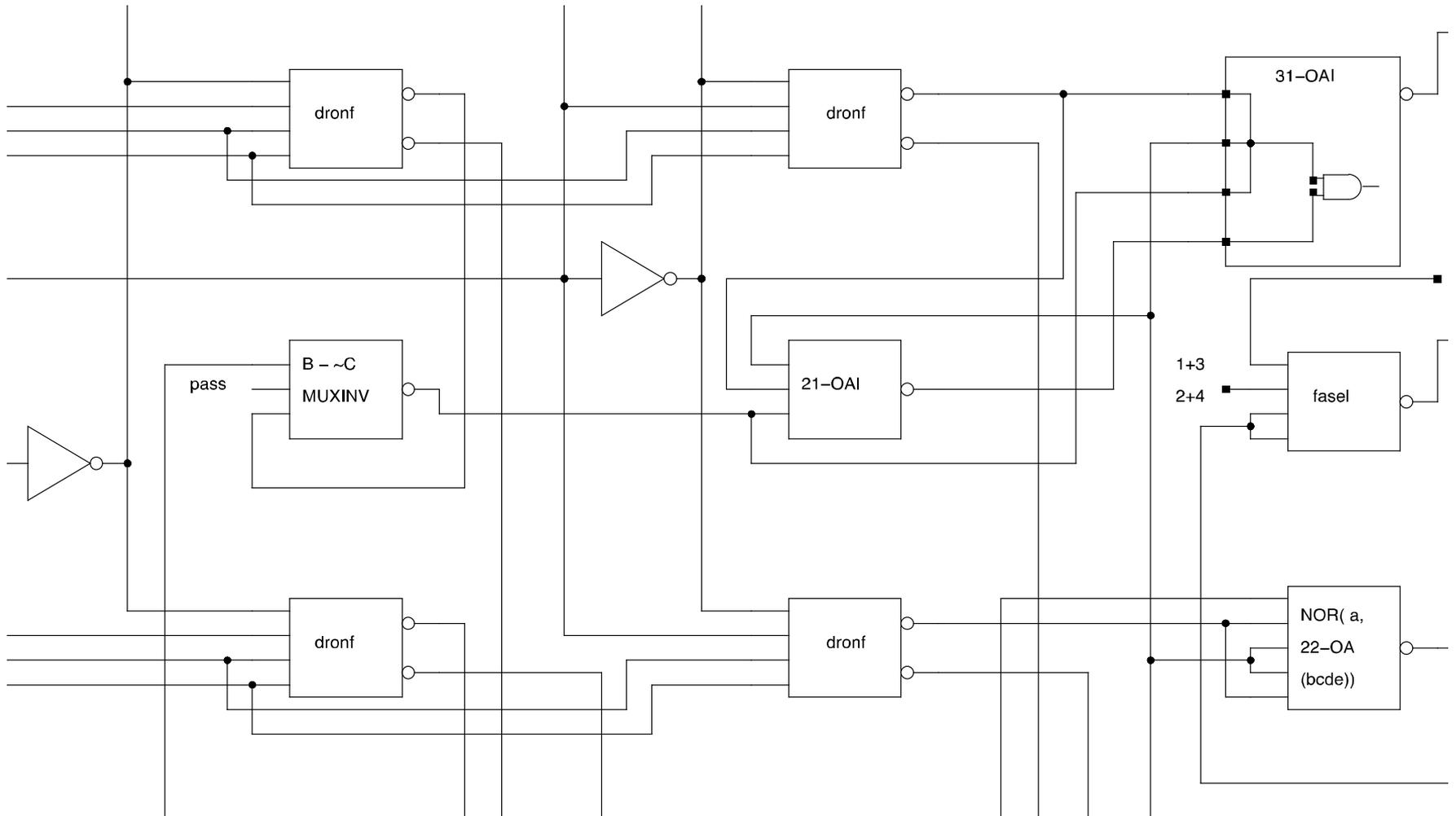
Port ID	Port Name	Port Description	In	Out
2384	!Q	!Q	<input type="checkbox"/>	<input checked="" type="checkbox"/>
2380	Q	Q	<input type="checkbox"/>	<input checked="" type="checkbox"/>
2388	clk	clk	<input checked="" type="checkbox"/>	<input type="checkbox"/>
2386	D	D	<input checked="" type="checkbox"/>	<input type="checkbox"/>
2382	rst	rst	<input checked="" type="checkbox"/>	<input type="checkbox"/>

Fill color: [Black swatch] Reset Color  
Frame color: [White swatch] Reset Color

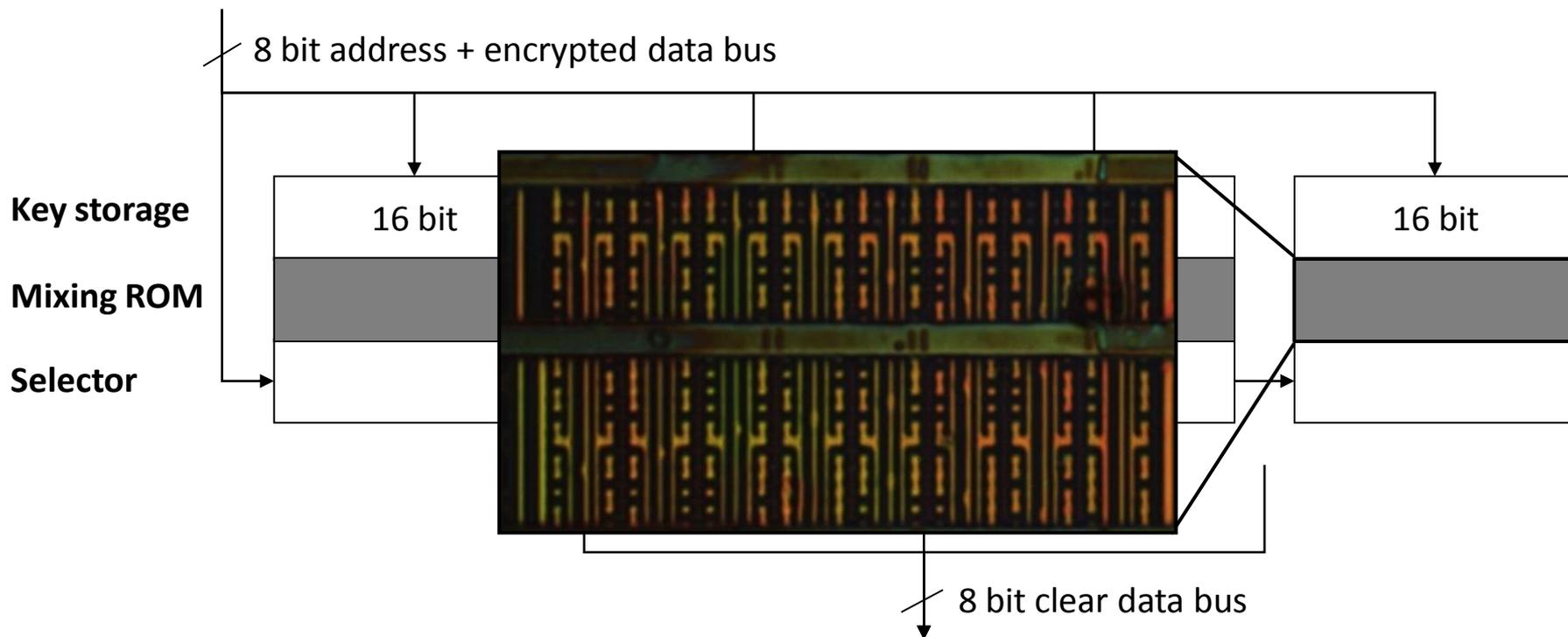
Buttons: Add, Remove, Cancel, OK

Autosaving project data ... done.

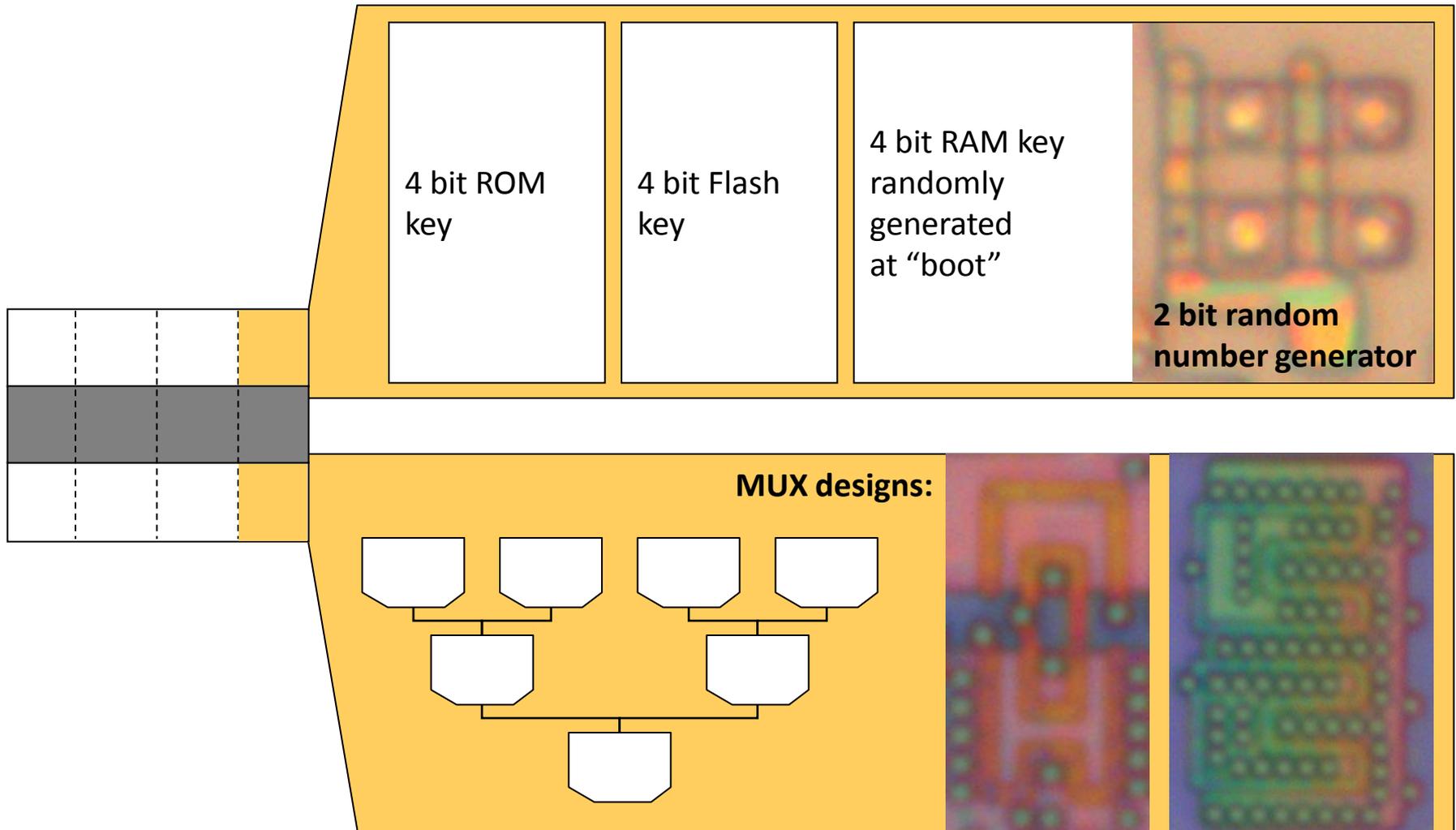
# Degate outputs synthesizable code that can be visualized with standard tools



# Memory is ciphered with 64 bit key



# Memory encryption includes non-deterministic and obfuscated cells



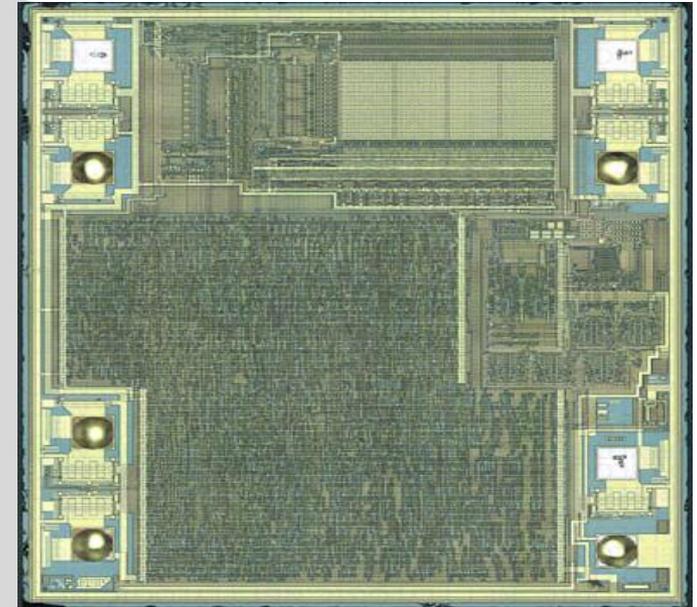
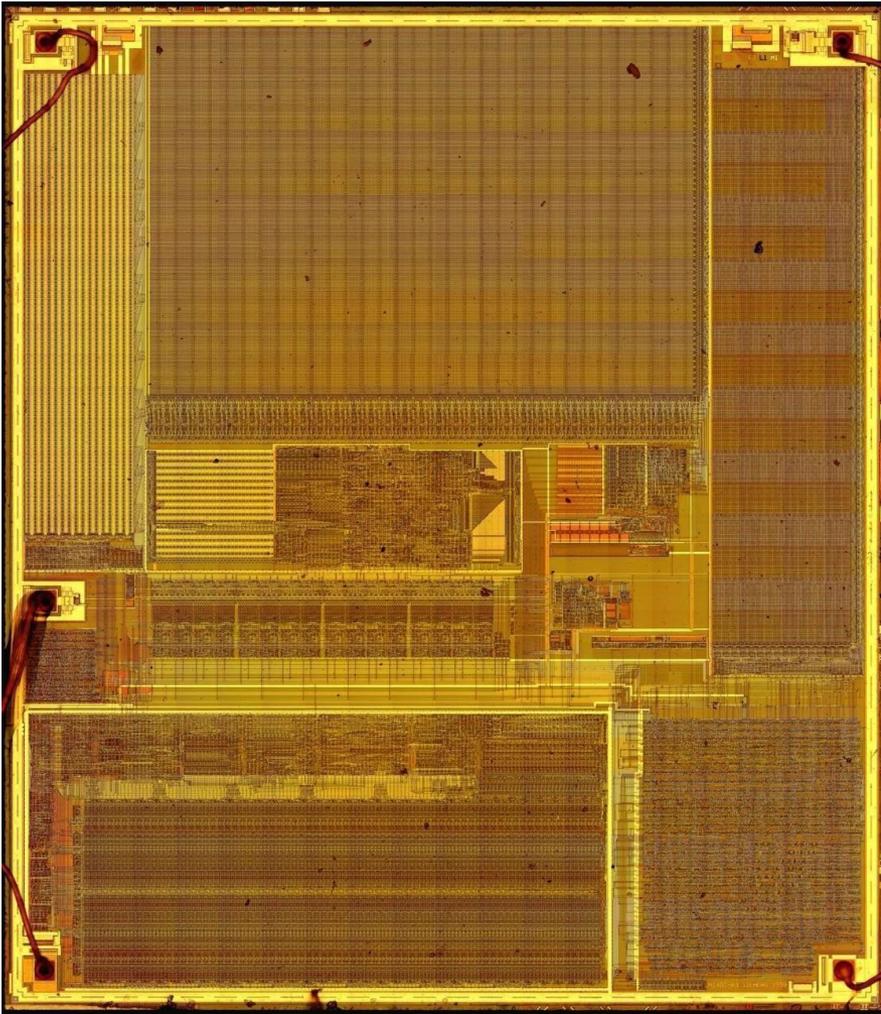
# Agenda

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- Smart card basics
  - Reverse-engineering memory encryption
  - **Mitigation measures**

# Hardening smart card systems requires actions from manufacturers and system designers

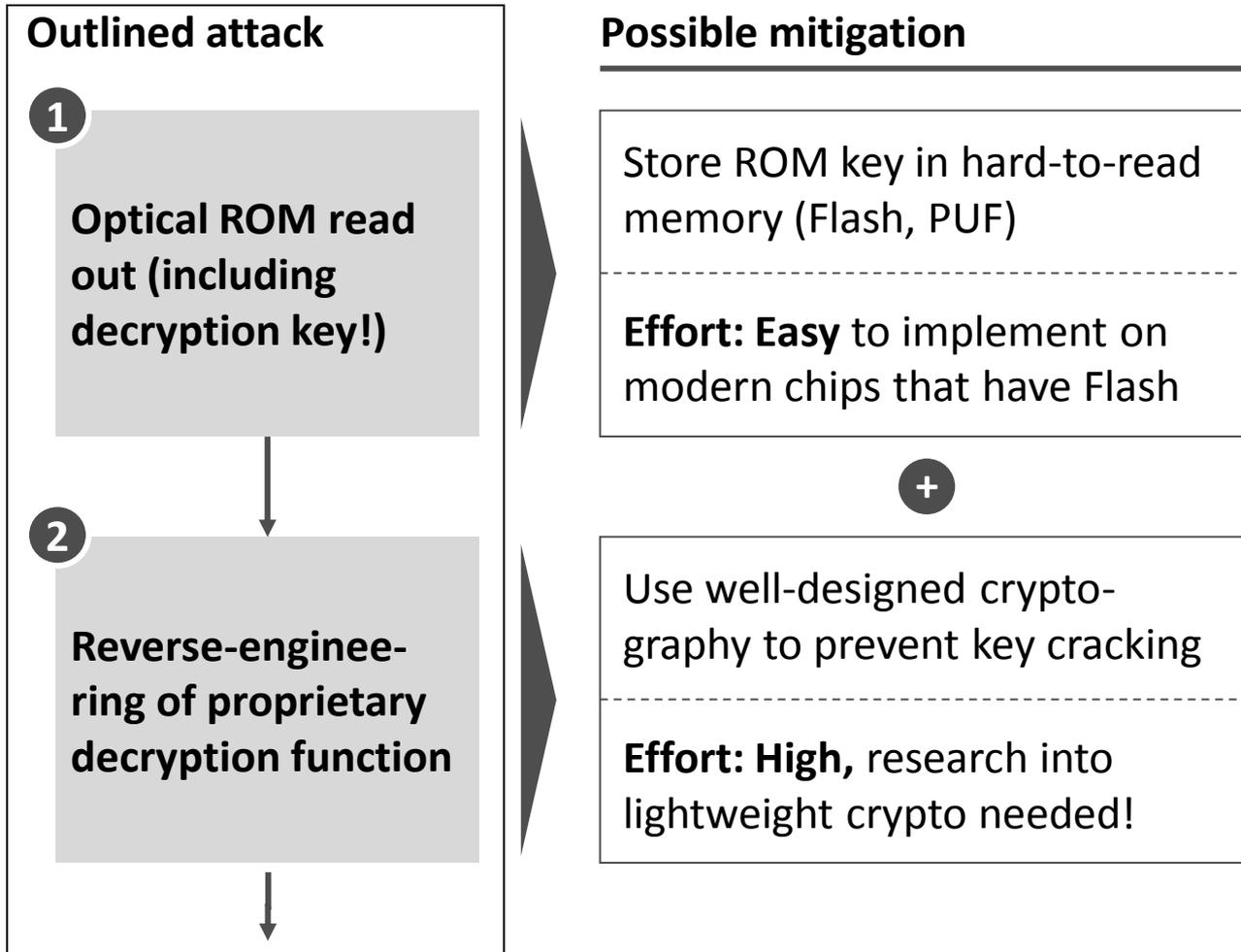
Mitigation step	Responsible
<b>A</b> Increase complexity of reverse-engineering	Smart card manufacturer
<b>B</b> Harden cipher against cryptanalysis	
<b>C</b> Keep smart card attack value low	System designer

**A** Best defense against reverse-engineering –  
Increase complexity, decrease feature size



- Use more random logic, separated in fewer blocks
- Make it harder to image chip (feature size <math><180\text{ nm}</math>)

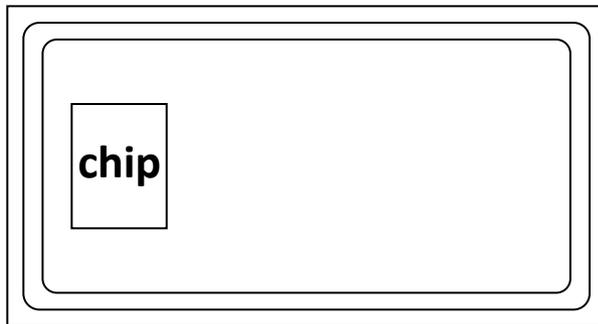
# B ROM code could be protected through better cryptography



# C Technology risks vary widely with use case

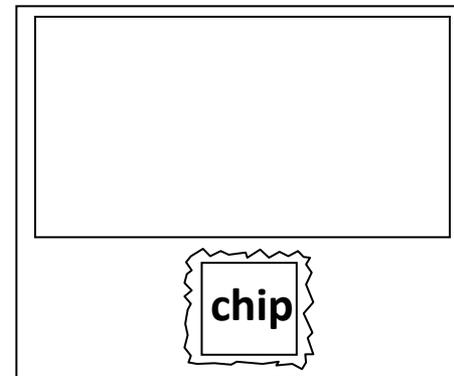
## Example: Nationwide micro-payment scheme

Payment card



Extracting secret keys  
allows cloning **one card**

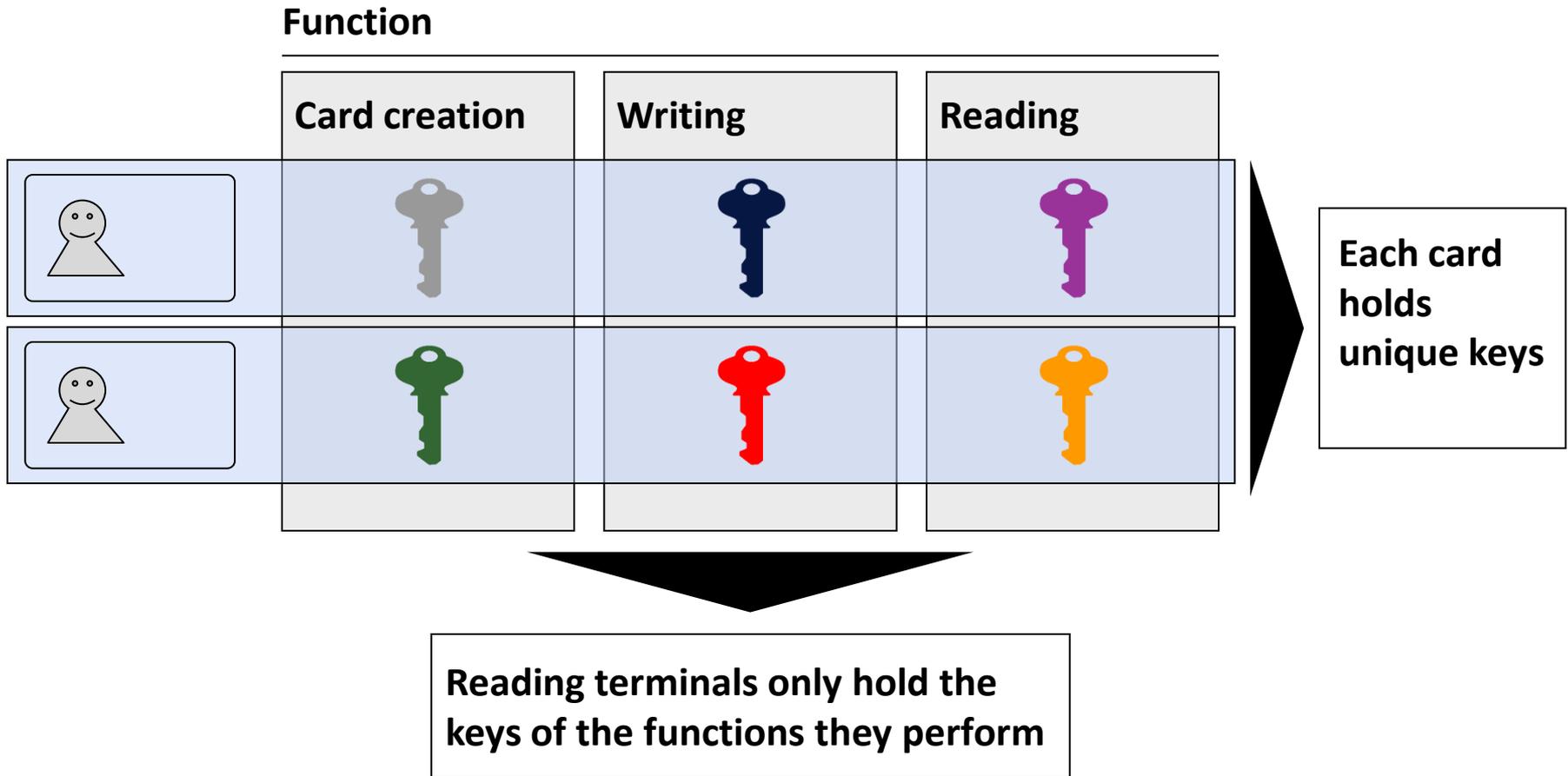
Payment terminal



Extracting secret keys  
allows cloning **all cards**

Same chip, same protection,  
but different security level

# C Key distribution should follow need-to-know principle to limit attack surface



# Smart card can provide large but not infinite level of protection

All smart cards can be reverse-engineered or broken with intrusive attacks at some cost

Software stored in ROM should be extractable for analysis from most modern smart cards

Smart cards are the most secure hardware, but system designers must limit attack incentives and not expect miracles from chips

**Degate software**, [degate.org](http://degate.org)  
**Silicon gate examples**, [siliconzoo.org](http://siliconzoo.org)

**Questions?**  
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